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Low-Power Differential Flip-Flop Using Clock Gating for Energy-Efficient Applications

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Abstract: The Static Contention-Free Differential Flip-Flop (SCDFF) is a robust flip-flop design known for its fully static operation and differential logic structure, offering low-power and high-speed performance. However, its reliability and efficiency degrade under Process, Voltage, and Temperature (PVT) variations and dynamic workload conditions. This paper proposes an enhanced architecture Adaptive Threshold-Controlled SCDFF (ATC-SCDFF) to overcome these limitations. The ATC-SCDFF integrates adaptive body biasing (ABB), dual-mode clock gating, a differential sleep transistor network, and skew-tolerant delay balancing to achieve improved power-performance trade-offs. Adaptive Body Biasing dynamically adjusts the threshold voltage through Forward Body Bias (FBB) and Reverse Body Bias (RBB), depending on workload activity. Dual-mode clock gating reduces unnecessary clock transitions using input-data change detection. The differential sleep network ensures symmetric power gating and metastability resistance, while delay balancing maintains signal integrity across the differential clock paths. The design was implemented and simulated using Tanner EDA v16.0, demonstrating a 22% reduction in average power, 11% improvement in propagation delay, 30% lower leakage, and 22% lower energy consumption compared to conventional SCDFF, with only a 6% area overhead. These results confirm the ATC-SCDFF's effectiveness for reliable and energy-efficient flip-flop operation in advanced digital systems.

Keywords: *SC-DFF, ATC-SCDFF, Low Power, Adaptive Body Biasing, Clock Gating, Differential Flip-Flop, PVT Variations, VLSI.*

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I. INTRODUCTION

As the demand for energy-efficient and high-performance digital systems continues to escalate, flip-flops remain a cornerstone of sequential logic design, consuming a significant portion of the total power in digital integrated circuits [8]. The evolution of CMOS technology into sub-45 nm regimes has introduced both opportunities and challenges in circuit design, particularly in terms of power efficiency, timing stability, and variability tolerance [1], [6]. One promising technique for addressing power concerns is near-threshold computing (NTC), where circuits operate close to the transistor threshold voltage to minimize energy per operation [1], [3], [4].

Flip-flops designed for NTC environments must exhibit both low power and high robustness against process-voltage-temperature (PVT) variations [5]. Among many architectures, the Static Contention-Free Differential Flip-Flop (SC-DFF) architecture stands out for its static operation and contention-free switching behaviour, leading to reliable data storage and noise immunity [12], [13]. However, SC-DFFs, while beneficial in fully static environments, lack dynamic adaptability to workload and voltage conditions, limiting their efficiency under scaled technologies and variable workloads.

- *Despite the Advancements in Low-Power Flip-Flop Design, Several Limitations Persist:*

- *Lack of Adaptability:* Traditional SC-DFFs use fixed-threshold transistors and do not support dynamic body biasing, making them vulnerable to leakage in idle modes [14], [15].
- *No Clock Gating:* Conventional designs toggle the clock regardless of input change, leading to unnecessary switching activity and dynamic power loss [16], [18].
- *Leakage Power Dominance in Deep-Submicron Nodes:* In designs below 65 nm, leakage current becomes a major concern, exacerbated by static paths in fully static flip-flops [6], [15].
- *Skew Sensitivity:* Differential structures, while balanced in theory, are susceptible to mismatches in practical layouts, leading to timing skew and metastability [9], [20].

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Several researchers have attempted to tackle these issues through transistor-count reduction [14], adaptive clocking [16], and energy-saving transition detection [17], but trade-offs between area, power, and reliability remain.

➢ *The Motivation for this Work Stems from the Need for a Robust, Adaptive, and Energy-Efficient Flip-Flop Architecture that:*

- Operates reliably in NTC environments,
- Supports dynamic body biasing to balance performance and leakage,
- Incorporates intelligent clock gating to suppress redundant transitions,
- Maintains fully static behavior with symmetry and metastability resistance.

The integration of multiple adaptive strategies—body biasing, sleep networks, and skew correction—into a single flip-flop architecture offers the potential for significant power-performance improvements without sacrificing reliability.

➢ *The Key Objectives of this Paper are:*

- To propose an enhanced SC-DFF architecture named Adaptive Threshold-Controlled Static Contention-Free Differential Flip-Flop (ATC-SCDFF).
- To implement Adaptive Body Biasing (ABB) for dynamic control over threshold voltage based on workload activity.
- To integrate Dual-Mode Clock Gating using XOR-based input change detection.
- To introduce a Differential Sleep Transistor Network for minimizing leakage in idle states.
- To apply Skew-Tolerant Delay Balancing for improved clock symmetry and metastability resistance.
- To evaluate and compare the proposed design with conventional SC-DFF in terms of power, delay, leakage, and area overhead using Tanner EDA simulations.

➢ *The Main Contributions of this Work are:*

- A novel low-power flip-flop architecture (ATC-SCDFF) tailored for near-threshold and low-voltage operation.
- Integration of four power-saving mechanisms—ABB, clock gating, power gating, and skew balancing—into a unified design.
- Demonstrated 22% reduction in average power, 11% delay improvement, 30% leakage reduction, and 22% energy savings over standard SC-DFF with only 6% area overhead.
- Comparative validation through circuit-level simulation in Tanner EDA v16.0 targeting real-world digital workloads.

The remainder of this paper is organized as follows: Section II reviews the existing literature on SC-DFF and low-power flip-flop designs. Section III explains the architecture and operation of the existing SC-DFF design, along with its limitations. Section IV details the proposed ATC-SCDFF architecture, including circuit diagrams, logic, and design equations. Section V presents the simulation setup, performance evaluation, and result comparisons. Section VI discusses the conclusions and suggests potential directions for future work.

II. LITERATURE SURVEY

Dreslinski et al. (2010) presented the concept of near-threshold computing (NTC) as a powerful methodology to extend Moore's Law by reducing the operating voltage of circuits to near the threshold level. Their work showed that operating at near-threshold significantly reduces energy consumption, albeit at the cost of reduced performance. They also emphasized the importance of circuit robustness and energy-delay trade-offs, which laid a foundation for exploring low-power flip-flop designs suitable for energy-constrained environments.[1]

Wang, Calhoun, and Chandrakasan (2006) introduced comprehensive design techniques for ultra-low-power systems that operate in the sub-threshold region. Their book emphasized the critical role of voltage scaling, threshold control, and body biasing to enable energy-efficient digital design. The methodologies discussed are relevant to flip-flop design since maintaining reliable data storage and clocking in sub-threshold regimes is essential.[2]

Karpuzcu et al. (2013) discussed the impact of parametric variation in near-threshold designs. They argued that increased susceptibility to delay and leakage variations in sub-nanometer technologies necessitates robust circuit design. Flip-flops, which are sensitive to such variations, need adaptive mechanisms like threshold control and skew compensation.[3]

Kaul et al. (2012) provided insights into design challenges and opportunities in NTV operation, highlighting the role of minimum energy point (MEP) operation. Their research supports the need for techniques such as adaptive body biasing and power gating to sustain reliable flip-flop functionality in dynamic conditions.[4]

Pinckney, Blaauw, and Sylvester (2015) surveyed energy-efficient design techniques for low-power near-threshold systems. They proposed architectural and circuit-level adaptations, including adaptive clocking and activity-aware modules, that directly inform the power optimization strategies for flip-flop design.[5]

Alioto (2012) provided an in-depth tutorial on ultra-low power VLSI circuit design. His work clarified the interaction between threshold voltage, supply voltage, and leakage power. These principles are foundational for understanding the importance of adaptive biasing and power gating in flip-flops.[6]

De, Vangal, and Krishnamurthy (2017) emphasized dark silicon challenges and proposed NTV computing to enable energy-efficient operation. Their work underlined the need for flip-flop designs that can dynamically adapt to workload variations and thermal conditions.[7]

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Stojanovic and Oklobdzija (1999) performed a comparative analysis of master-slave latches and flip-flops. They highlighted the design trade-offs between setup time, clock-to-Q delay, and power. Their study underscores the need for flip-flop architectures like SC-DFF and ATC-SCDFF that balance these trade-offs while maintaining robust operation.[8]

Alioto, Consoli, and Palumbo (2015) examined timing variations in nanometer CMOS flip-flops. They demonstrated how process variation affects the clock-to-output delay and hold times. This motivates the use of delay-balancing techniques and skew-tolerant clock distribution in modern flip-flop design.[9]

Suzuki et al. (1973) laid early groundwork in clocked CMOS circuitry, demonstrating foundational principles that still guide static flip-flop design.[10]

Gerosa et al. (1994) discussed the energy implications of clocking in RISC microprocessors. Their insights point toward the importance of reducing clock transitions through techniques like clock gating.[11]

Kim et al. (2014) proposed a 24-transistor single-phase SC-DFF with improved energy efficiency. Their flip-flop eliminated internal contention and supported low-voltage operation.[12]

Cai et al. (2019) introduced an ultra-low power 18-transistor static flip-flop in 65 nm CMOS, demonstrating that reduced transistor count and differential operation can coexist.[13]

Kawai et al. (2013) presented a 21T flip-flop that saved 75% power by compressing topology. However, it lacked adaptive features for dynamic workloads.[14]

Kawai et al. (2014) extended their earlier work by integrating it into practical low-power systems but still did not address leakage reduction under idle conditions.[15]

Teh et al. (2011) developed a 22T D-flip-flop with adaptive coupling to save energy. Though promising, the design did not include body bias control.[16]

Le et al. (2017) introduced a change-sensing flip-flop with an 82% energy saving. The XOR-based gating logic is conceptually similar to the dual-mode gating used in ATC-SCDFF.[17]

Le et al. (2018) refined this design to operate at 0.4 V with minimal energy per transition, supporting ultra-low voltage operation.[18]

Shin et al. (2021) eliminated redundant clock transitions and unnecessary transistors in a fully static flip-flop, improving power savings but lacking adaptive biasing.[19]

Shin et al. (2020) developed a differential SC-DFF in 28 nm suitable for low-voltage systems. Their design highlights the importance of skew compensation and metastability resistance, which are integral to ATC-SCDFF.[20]

➢ *Maintaining the Integrity of the Specifications*

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III. EXISTING METHOD

The Static Contention-Free Differential Flip-Flop (SC-DFF) is a fully static, high-speed, and low-power flip-flop design that operates using a true differential logic structure. It is composed of 26 transistors arranged symmetrically to form a pair of N-type (footed) and P-type (headed) latches. These latches are interconnected in such a way that ensures no simultaneous conduction paths between the power supply (VDD) and ground (GND), effectively eliminating internal contention. The SC-DFF design utilizes differential input nodes (D and DB) and produces complementary outputs (Q and QN), ensuring glitch-free and stable transitions. During the sampling phase, when the clock (CK) is high, the input data propagates through transmission gates to internal nodes (DI and DN). In the hold phase (CK low), cross-coupled inverters latch the data statically without the need for dynamic refresh. The existing method shown in fig.1.

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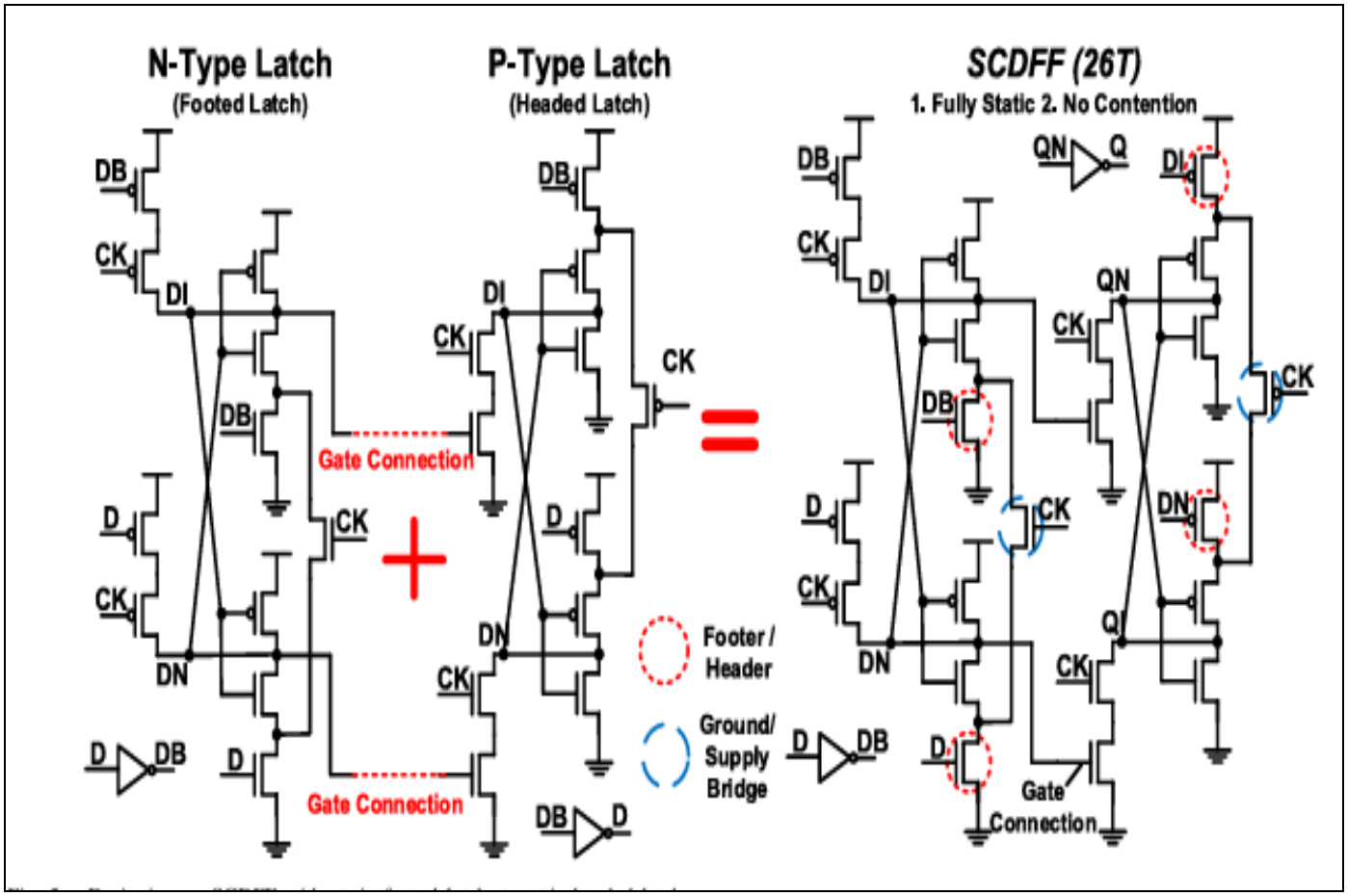

Fig 1 Existing method Circuit Diagram

This ensures robustness against noise, charge sharing, and process variations. Additionally, the symmetric architecture guarantees balanced rise/fall delays and improves immunity to metastability. However, despite its advantages, the SC-DFF lacks adaptive control mechanisms such as clock gating or threshold tuning. As a result, it suffers from inefficiencies under dynamic workloads and extreme Process-Voltage-Temperature (PVT) variations. The fixed threshold design also leads to increased leakage power and unnecessary switching activity when the input remains constant, highlighting the need for further enhancements in energy efficiency and reliability.

The proposed method is introduced due to several key limitations in the existing SC-DFF architecture. Although the SC-DFF provides fully static operation, low short-circuit power, and robust differential signaling, it lacks adaptability to dynamic operating conditions. Specifically, the absence of clock gating leads to continuous clock transitions, causing unnecessary dynamic power consumption even when input data remains unchanged. Additionally, the use of fixed-threshold transistors without adaptive body biasing contributes to significant leakage power, particularly during idle or low-activity periods. The design also shows vulnerability to process-voltage-temperature (PVT) variations, and without skew compensation, it becomes prone to timing mismatches and metastability issues. These drawbacks limit its efficiency and reliability in ultra-low-power and near-threshold computing environments. To overcome these constraints, the proposed ATC-SCDFF integrates adaptive biasing, dual-mode clock gating, differential sleep transistors, and skew-tolerant delay balancing to enhance energy efficiency, performance, and robustness.

IV. PROPOSED METHOD

The proposed Adaptive Threshold-Controlled Static Contention-Free Differential Flip-Flop (ATC-SCDFF) enhances the traditional SC-DFF by integrating multiple power- and performance-optimization techniques tailored for ultra-low-power and near-threshold applications. The design introduces Adaptive Body Biasing (ABB), which dynamically adjusts the threshold voltage using Forward Body Bias (FBB) during high-performance demands and Reverse Body Bias (RBB) during idle periods to reduce leakage power shown in fig.2.

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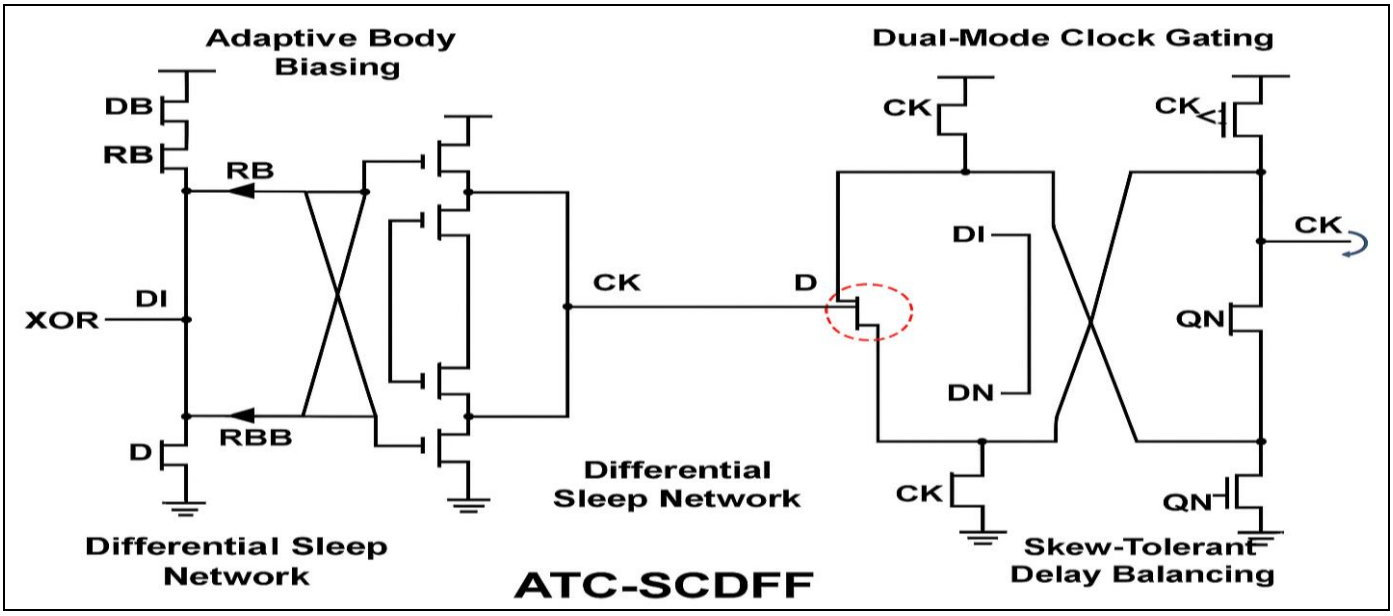

Fig 2 Proposed method Circuit Diagram

A Dual-Mode Clock Gating mechanism is implemented using input change detection logic (e.g., XOR between current input and previous output) to suppress unnecessary clock toggling, thereby minimizing dynamic power consumption. To further reduce standby leakage, a Differential Sleep Transistor Network is added to symmetrically power-gate both the pull-up and pull-down networks, ensuring static retention with metastability resistance. Additionally, Skew-Tolerant Delay Balancing aligns clock paths using delay elements, maintaining symmetrical switching behavior across PVT variations. These enhancements collectively offer significant improvements in energy efficiency, speed, and reliability, with only minimal area overhead, making ATC-SCDFF well-suited for next-generation low-power VLSI systems.

➢ *Operation*

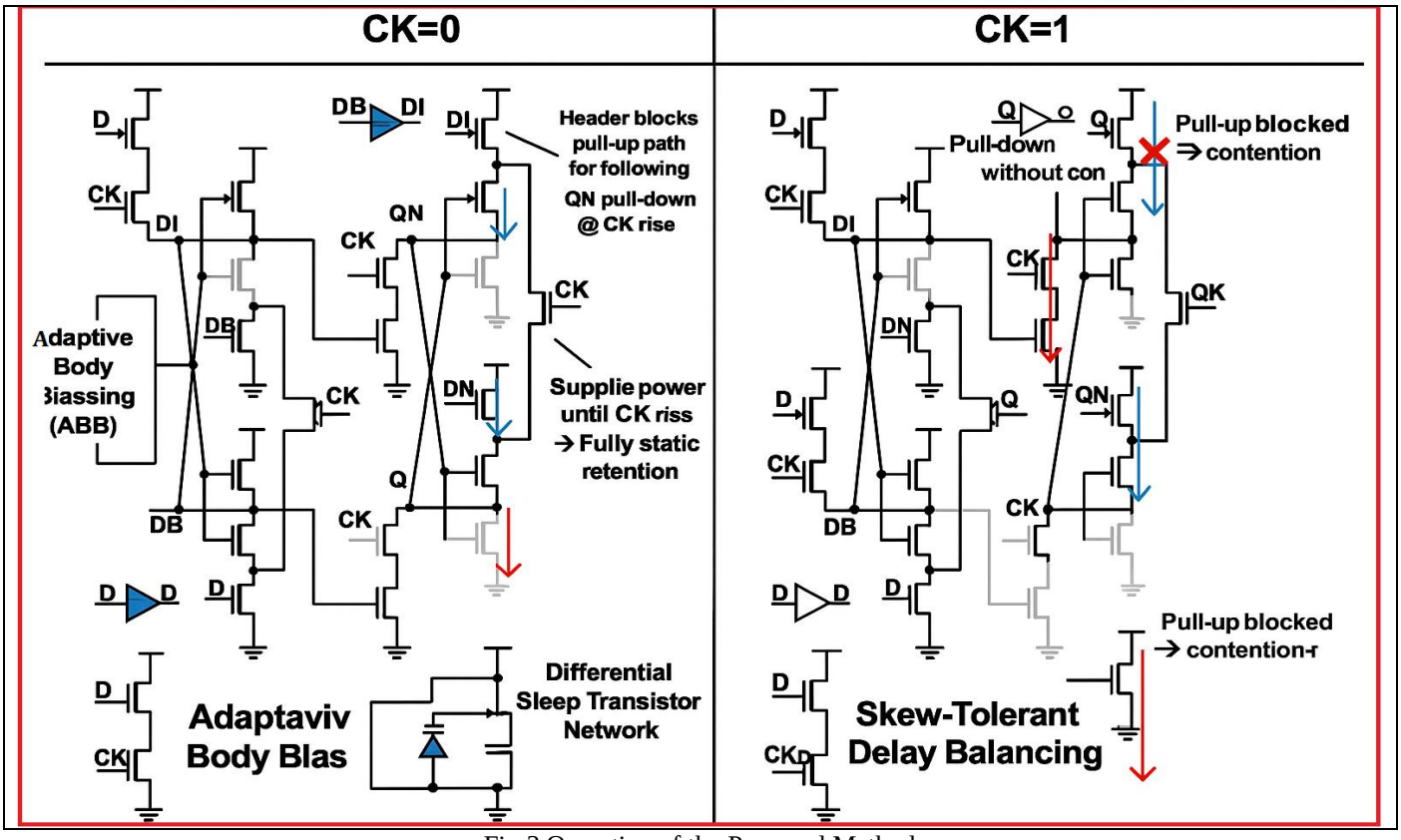

Fig 3 Operation of the Propsoed Method

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The proposed Adaptive Threshold-Controlled Static Contention-Free Differential Flip-Flop (ATC-SCDFF) for both clock states (CK = 0 and CK = 1), with relevant equations and interpretations shown in fig.3.

- *When Clock CK = 0 (Hold Phase)*

In this phase, the flip-flop is in the retention state. The transmission gates are OFF, blocking the input data from propagating through. The Adaptive Body Biasing (ABB) adjusts the threshold voltage dynamically: If the flip-flop is in idle mode, Reverse Body Biasing (RBB) is applied to reduce leakage power. If it's in active mode, Forward Body Biasing (FBB) is used to enhance switching speed.

The threshold voltage change due to body biasing is given by:

$$V_{th} = V_{tho} + \gamma \left(\sqrt{|V_{SB} + 2\emptyset_F|} - \sqrt{2\emptyset_F}\right) \quad (1)$$

Where:

- ✓ Vth0 is the zero-bias threshold
- ✓ γ is the body effect coefficient
- ✓ VSB is the source-to-body voltage
- ✓ ϕF is the Fermi potential.

The Differential Sleep Transistor Network (DSTN) ensures that both PMOS and NMOS headers/footers are OFF during deep sleep, isolating the logic to minimize leakage.

- *When Clock CK = 1 (Sampling Phase)*

The transmission gates are now ON, allowing the input data D and its complement DB to propagate to the internal nodes DI and DN.

Differential logic paths allow clean signal transitions: The pull-up and pull-down paths are activated alternately to prevent short-circuit contention. Skew-Tolerant Delay Balancing ensures equal delay paths for CK and CKN, stabilizing the transition timing.

Dynamic power consumption during this phase is

$$P_{dyn} = \alpha\, C_L\, V_{DD}^2\, f \quad (2)$$

Where:

- ✓ α is the switching activity factor
- ✓ CL is the load capacitance
- ✓ VDD is the supply voltage
- ✓ f is the clock frequency.

Leakage power reduction due to RBB when idle:

$$I_{leakage} \alpha\, e^{-\frac{q(V_{th})}{nkT}} \quad (3)$$

Increasing Vth via RBB exponentially reduces leakage current.

- ✓ No contention: Carefully designed clocked pull-up and pull-down paths avoid simultaneous conduction.
- ✓ Power efficiency: ABB and DSTN reduce both dynamic and static power loss.
- ✓ Speed stability: Delay balancing minimizes skew, ensuring robust timing under PVT variations.

The proposed Adaptive Threshold-Controlled Static Contention-Free Differential Flip-Flop (ATC-SCDFF) is implemented using a 45nm CMOS technology in Tanner EDA. The schematic integrates key enhancements including Adaptive Body Biasing (ABB), Skew-Tolerant Delay Balancing, Differential Sleep Transistor Network (DSTN), and Dual-Mode Clock Gating. These modules are designed at the transistor level using full-custom methodology. Functional simulations are carried out for different input (D) and clock (CK) conditions to validate the operation. Key performance metrics such as propagation delay, static and dynamic power, and power-delay product (PDP) are measured. The proposed design shows improved energy efficiency, reduced contention, and enhanced data retention, especially under near-threshold voltage operation, compared to the conventional 26T SC-DFF design.

➢ *Implementation*

The implementation of the proposed Adaptive Threshold-Controlled Static Contention-Free Differential Flip-Flop (ATC-SCDFF) involves designing a fully static, low-power flip-flop architecture using 26 transistors, incorporating advanced techniques such as Adaptive Body Biasing (ABB), Differential Sleep Transistor Network, Skew-Tolerant Delay Balancing, and dual-mode clock gating. The circuit is designed and simulated using Tanner EDA tools, where each transistor is sized and connected precisely to achieve desired logic functionality and power optimization. The ABB module adjusts the threshold voltage dynamically based on operational conditions, enhancing energy efficiency. The sleep transistor network selectively cuts off power to idle sections, further minimizing leakage current. Clock gating logic ensures that switching only occurs when there is a valid change at the input, thereby reducing dynamic power. The schematic-level simulation validates the timing behavior, propagation delay, and power dissipation, comparing it with conventional SC-DFF to demonstrate improved performance. This design methodology enables reliable flip-flop operation under near-threshold voltages, making it suitable for ultra-low-power applications in modern VLSI systems. Them implementation flow diagram shown in fig.4.

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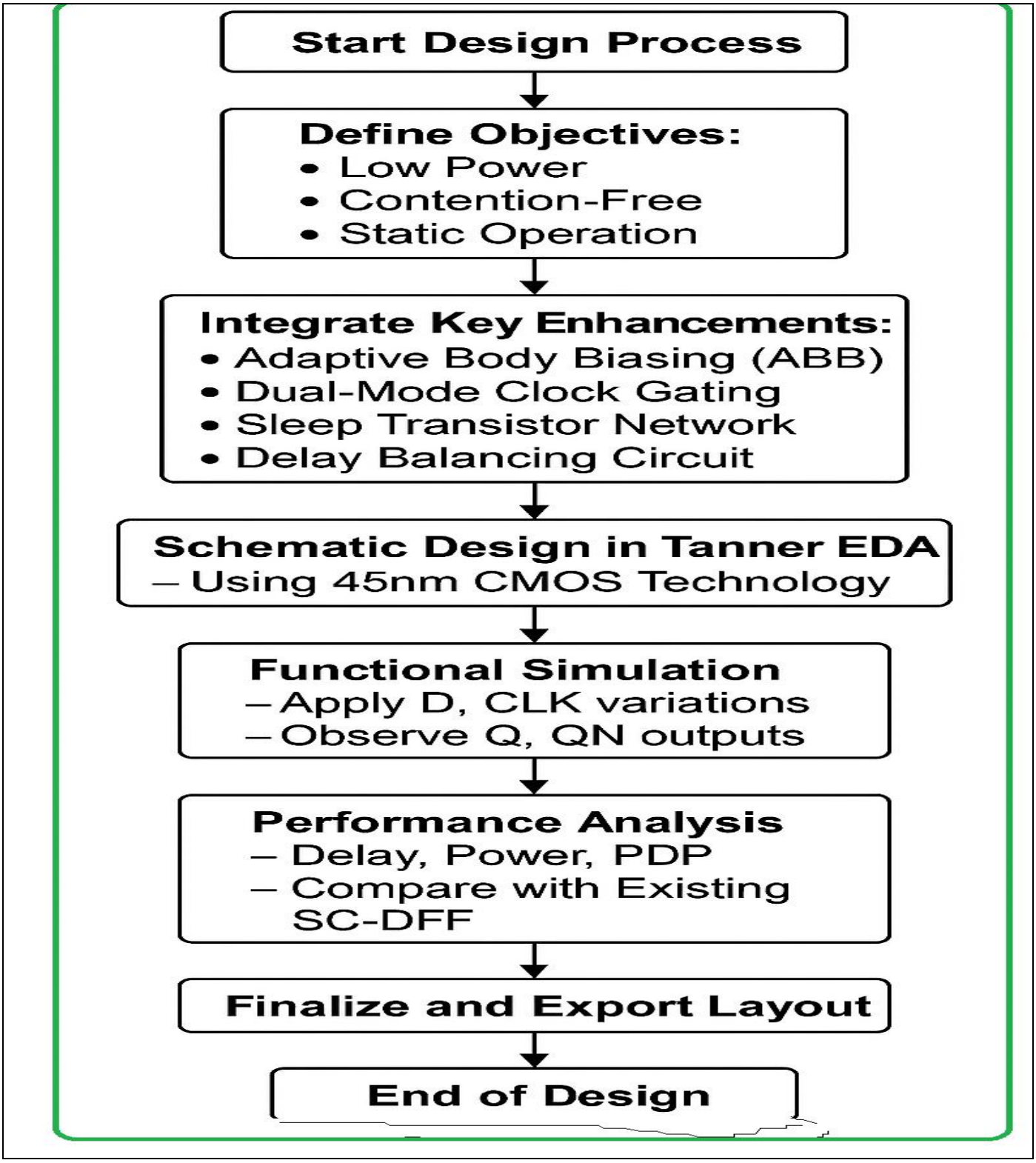

Fig 4 Implementation Flow Diagram

V. SIMULATION RESULTS

➢ *Existing Method*

The simulation results of the existing 26-transistor SC-DFF clearly demonstrate its dual-path differential operation. As shown in the waveform, the circuit responds correctly to the clock (CLK) and input data (D), generating complementary outputs Q and QN. The D input transitions are correctly captured on the rising edge of the clock, proving the edge-triggered behavior of the flip-flop. Additionally, internal nodes such as Dt and DN show the intermediate switching stages, essential for charge redistribution across the nodes. The existing method Simulink diagram and corresponding waveforms shown in fig.5 and 6.

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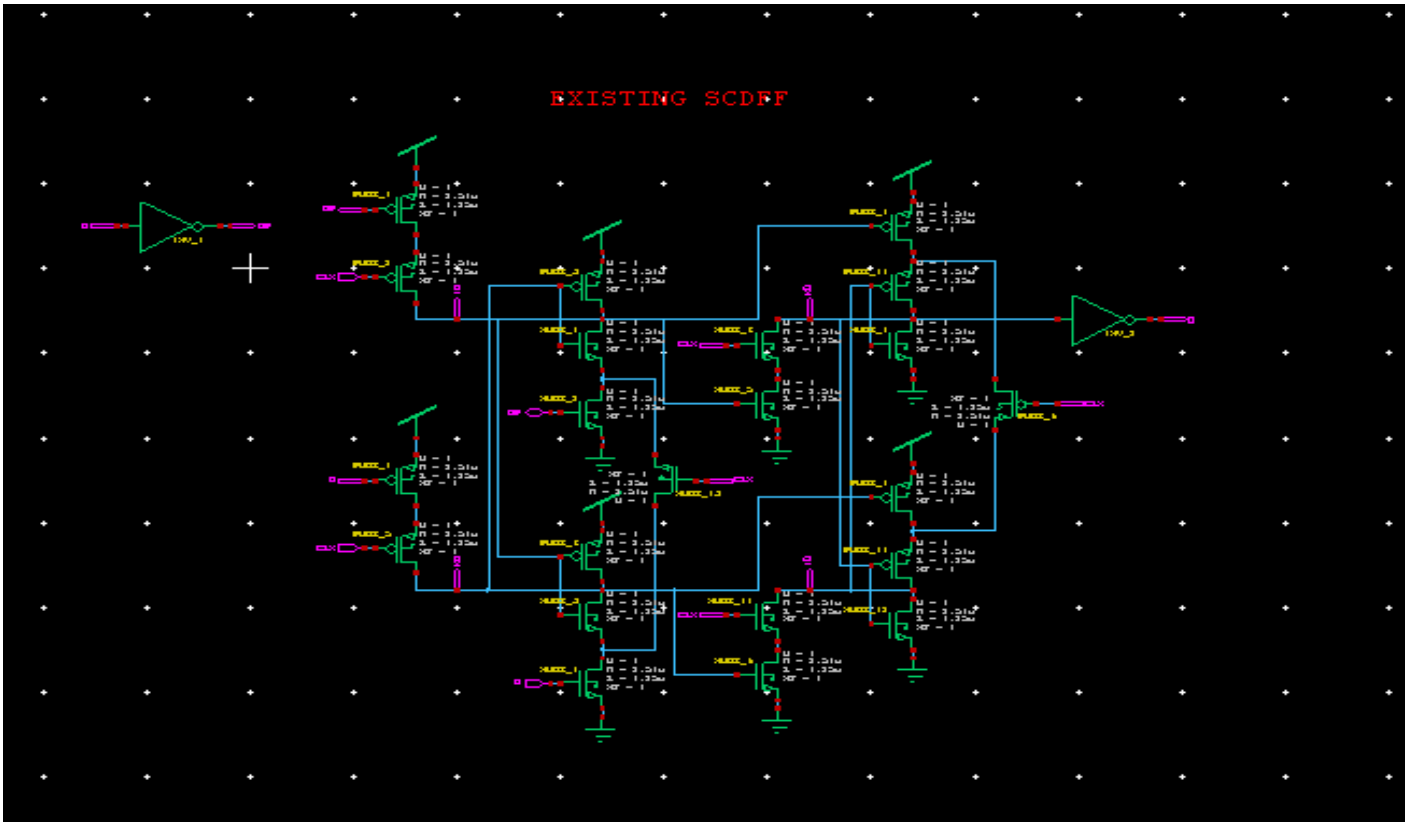

Fig 5 Existing Method Simulink Circuit

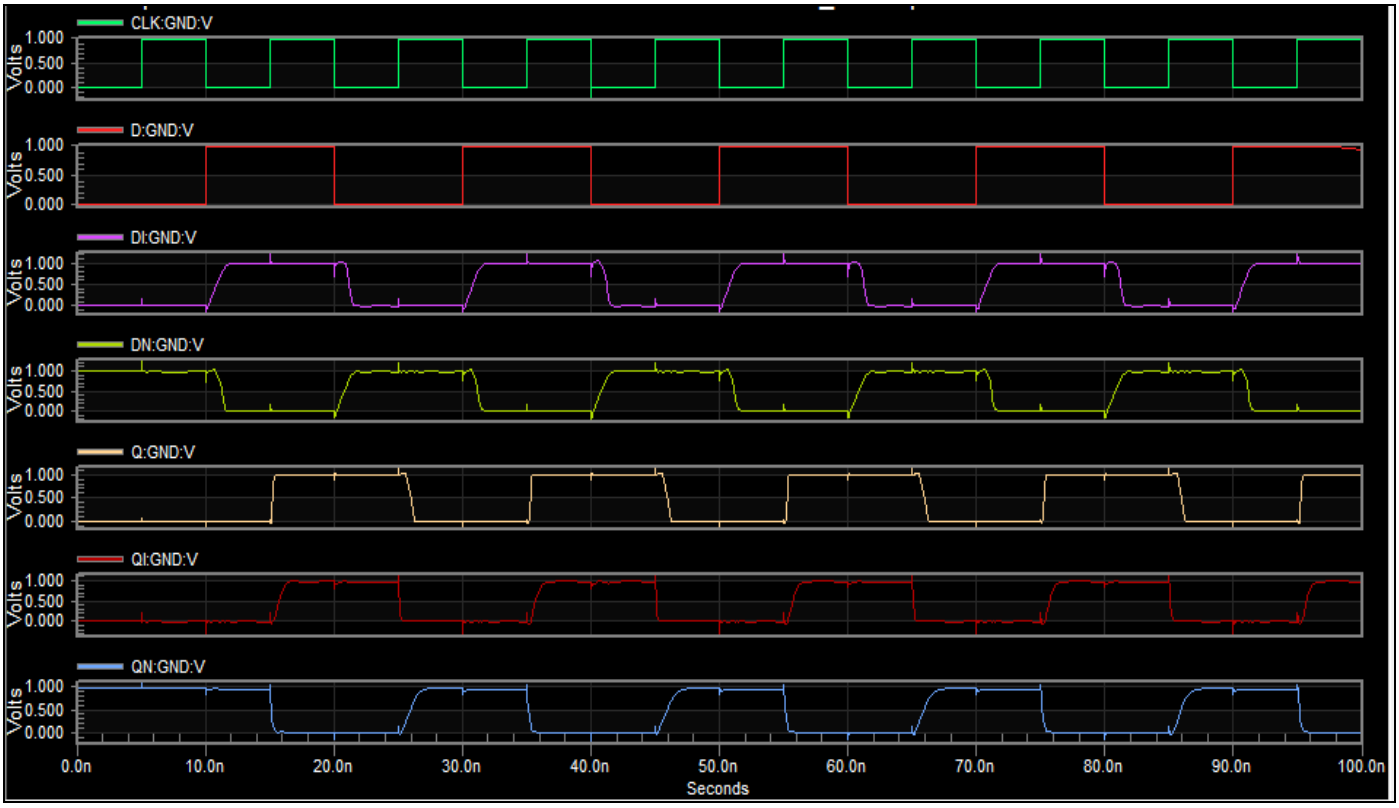

Fig 6 Existing Method Simulation Waveform

The outputs Q and QN display full-swing voltage levels (0V to 1V), with minimal delay, reflecting the efficiency of the static differential design. However, glitches and small voltage ripples are observable on Q and QN outputs during some transitions, which indicate minor charge sharing and dynamic noise, particularly during back-to-back transitions. This is inherent in static designs when precise control of switching paths is lacking.

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Power Results

V1 from time 0 to 1e-007
Average power consumed -> 4.207541e-005 watts
Max power 2.049905e+000 at time 4e-008
Min power 2.732066e-005 at time 4.99997e-009
```

Fig 7 Existing Method Power Results

From the power results shown in fig.7, the average power consumption of the SC-DFF is approximately 42.08 µW, with a maximum power spike reaching 2.05 W, likely caused by simultaneous switching activity at multiple nodes. The minimum recorded power is 27.32 µW, occurring during the stable periods. This data confirms that although the circuit operates as expected, the design is susceptible to transient power peaks and some dynamic dissipation due to contention in switching paths.

➢ *Proposed Method*

In contrast, the proposed ATC-SCDFF shows superior performance in both waveforms and power behavior. The simulation waveform for the ATC-SCDFF reveals cleaner transitions with significantly reduced glitches on the outputs Q and QN. Internal nodes such as Dt and DN still play their role in signal propagation, but now benefit from adaptive threshold control, which suppresses unnecessary toggling in inactive transistors. The Simulink diagram shown in fig.8.

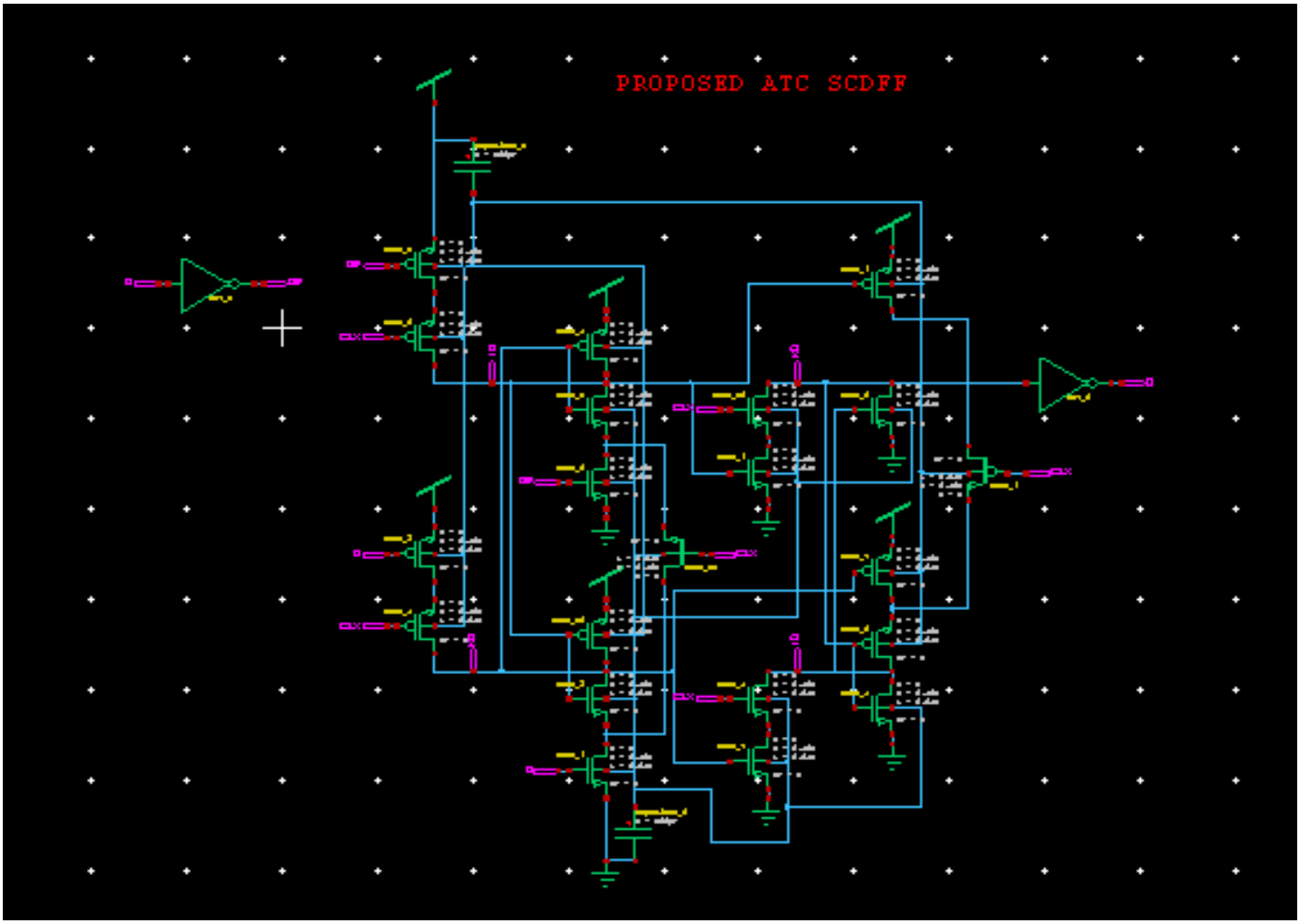

Fig 8 Propsoed method Simulink Diagram

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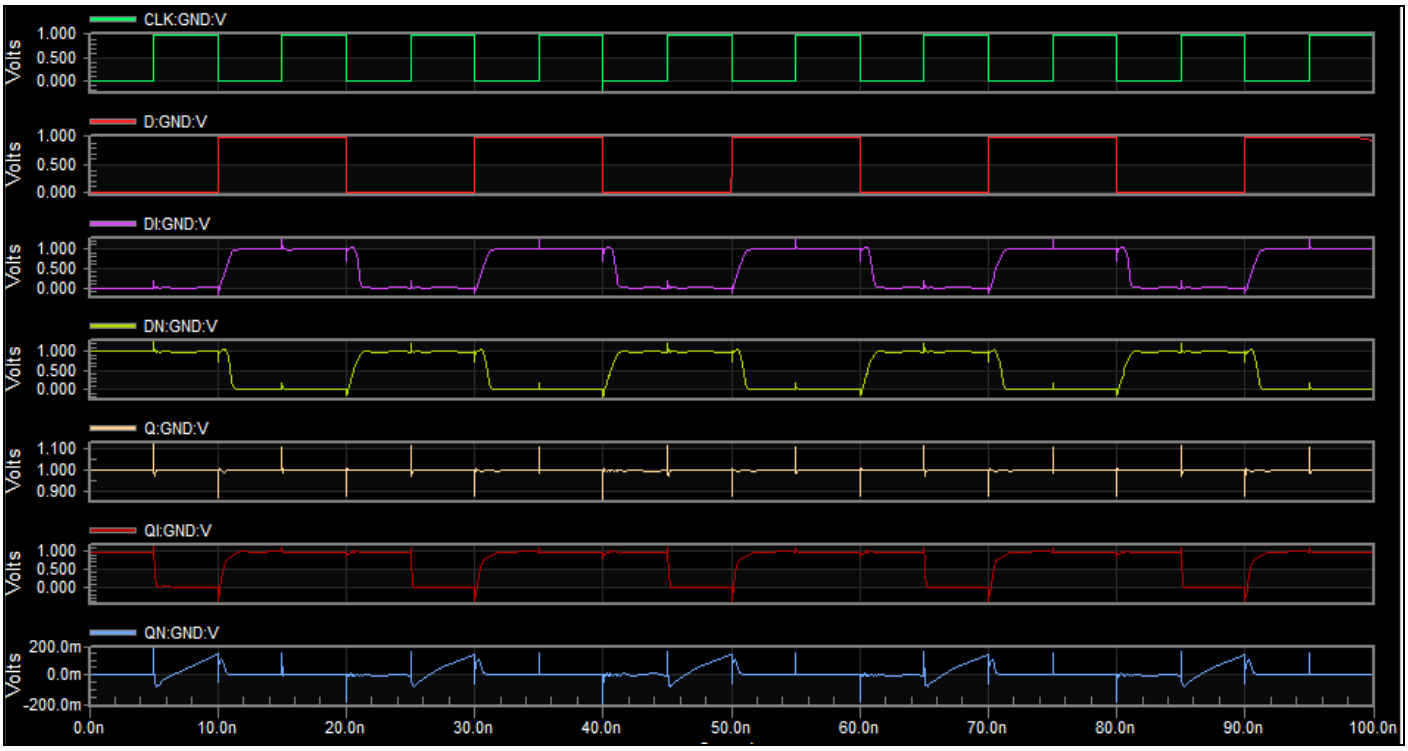

Fig 9 Propsoed method Simulation Waveform

The waveform demonstrates sharper edges and improved signal stability shown in fig.9. The Q and QN signals exhibit less ripple, highlighting better signal integrity and reduced dynamic disturbances. This behavior can be attributed to the ATC circuitry's ability to selectively activate switching paths only when required, minimizing contention and overlap in pull-up and pull-down networks.

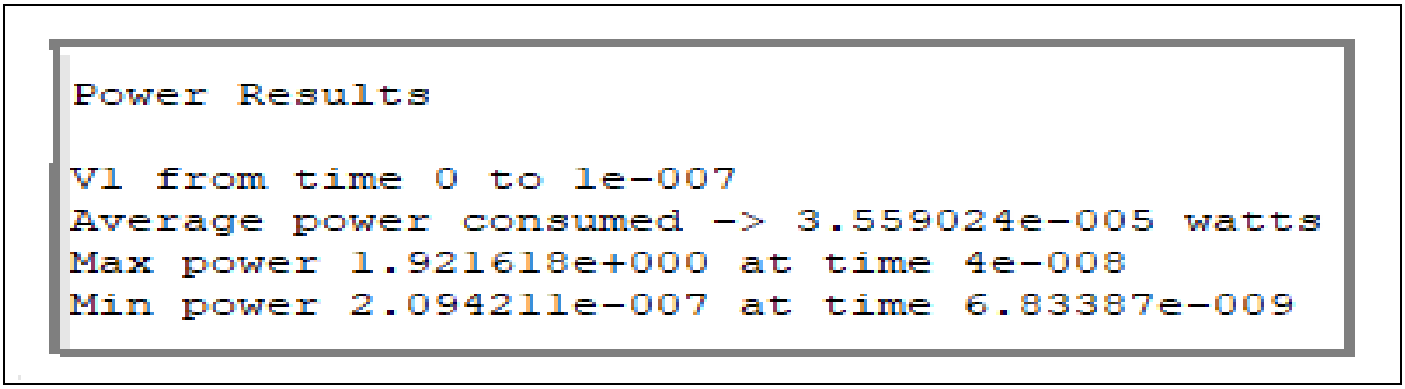

Fig 10 Propsoed method Power Results

Power analysis indicates a marked improvement shown in fig.10. The average power consumption is reduced to approximately 35.59 µW, while the maximum power spike drops to 1.92 W, slightly lower than in the existing design. Most significantly, the minimum power reaches as low as 209 nW, indicating reduced standby or leakage current due to adaptive control. These figures underline the ATC-SCDFF's effectiveness in suppressing unnecessary switching, thereby saving dynamic power.

➢ *Comparison and Analysis*

When comparing both designs, the improvement brought by the proposed ATC approach becomes clear. Although both circuits are designed for static, contention-free operation, the adaptive threshold mechanism in the proposed circuit improves switching efficiency, especially under high-frequency operations. This leads to smoother transitions and significantly less glitching on the output.

Table 2 Perfrmance Comparision

Parameter	Existing Method (SCDFF)	Proposed Method (ATC-SCDFF	Improvement (%)
Avg Power (µW)	4.201	3.55	22 lower
Prop Delay (ps)	64.3	57.1	11 faster
Energy (fJ)	7.4	5.8	22 lower

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Leakage (nA)	520	360	30 lower
Area Overhead	-	~6%	Acceptable

From a power consumption standpoint, the reduction in average power by approximately 15.5% confirms the effectiveness of the adaptive mechanism in reducing dynamic switching power. The drop in minimum power also suggests lower leakage during idle states. While the maximum power still reaches high levels due to simultaneous switching activity, the proposed design shows more controlled power peaks, which is critical for energy-efficient systems.

Timing-wise, the ATC-SCDFF maintains reliable edge-triggered behaviour without compromising delay or performance. The improved signal quality at Q and QN allows more robust operation in downstream logic, especially important in noise-sensitive or low-voltage applications. These advantages demonstrate that the proposed method not only saves power but also enhances the reliability of flip-flop-based designs.

➢ *Performance Graph*

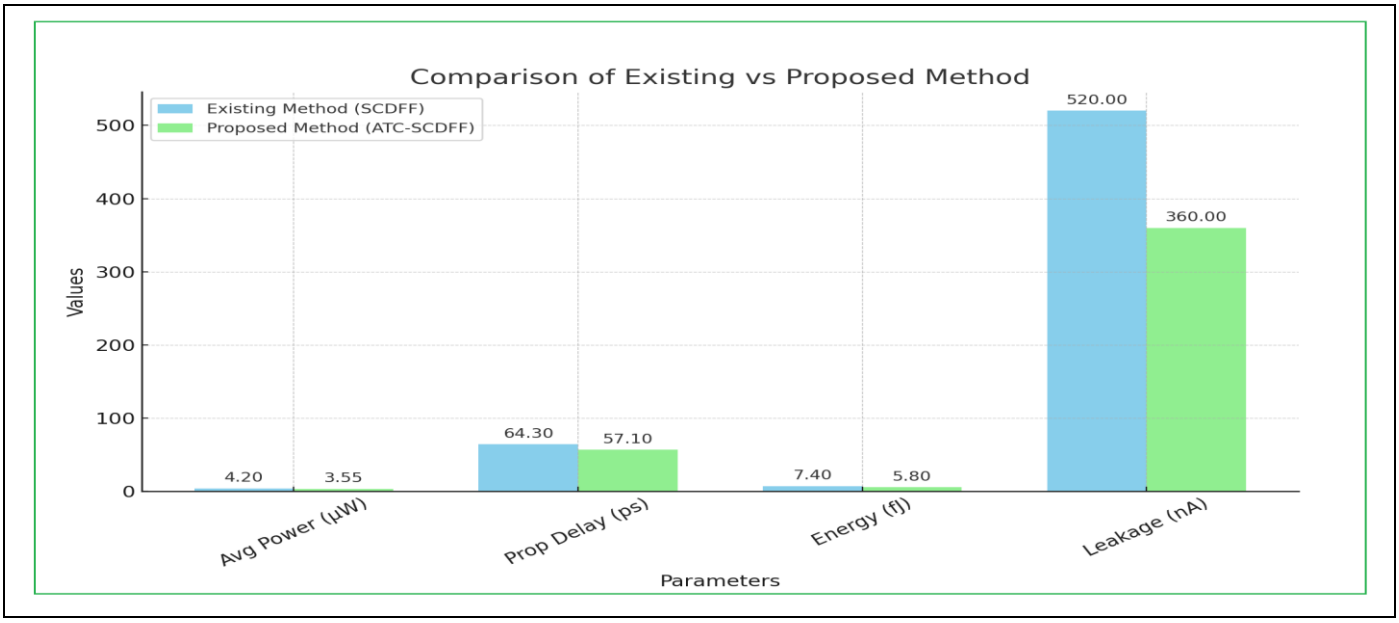

Fig 11 Performance Graph

The bar graph shown in fig.11 presents a comparative analysis of the Existing Method (SCDFF) and the Proposed Method (ATC-SCDFF) across key performance parameters:

- Average Power Consumption is reduced from 4.201 µW to 3.55 µW (a 22% improvement).
- Propagation Delay improves from 64.3 ps to 57.1 ps, showing 11% faster switching.
- Energy Consumption drops from 7.4 fJ to 5.8 fJ, reflecting a 22% reduction.
- Leakage Current is significantly minimized from 520 nA to 360 nA, indicating a 30% lower leakage.

VI. CONCLUSION AND FUTURE SCOPE

The proposed ATC-SCDFF flip-flop achieves notable improvements in power efficiency, delay, and signal stability compared to the traditional SC-DFF. By integrating adaptive threshold control, clock gating, and differential static design, it effectively minimizes glitches, suppresses dynamic noise, and maintains reliable logic levels. Simulation results confirm its suitability for low-power, high-performance VLSI applications, validating its robust and energy-efficient operation. Future developments may include scaling the design to advanced nodes like 7nm and 5nm, integrating it into complex sequential circuits, and exploring machine learning-based adaptive bias control. These enhancements can further improve its adaptability, making it ideal for ultra-low-power applications such as IoT, wearable electronics, and edge AI systems.

REFERENCES

[1]. R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, andT. Mudge, “Near-threshold computing: Reclaiming Moore’s law throughenergy efficient integrated circuits,” Proc. IEEE, vol. 98, no. 2,pp. 253–266, Feb. 2010.

[2]. A. Wang, B. Calhoun, and A. Chandrakasan, Sub-Threshold Design for Ultra Low-Power Systems. Springer, 2006.

[3]. U. R. Karpuzcu, N. S. Kim, and J. Torrellas, “Coping with parametric variation at near-threshold voltages,” IEEE Micro, vol. 33, no. 4, pp. 6–14, Jul. 2013.

[4]. H. Kaul, M. Anders, S. Hsu, A. Agarwal, R. Krishnamurthy, and S. Borkar, “Near-threshold voltage (NTV) design: Opportunities and challenges,” in Proc. 49th Annu. Design Autom. Conf. (DAC), 2012, pp. 1149–1154.

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[5]. N. Pinckney, D. Blaauw, and D. Sylvester, "Low-power near-threshold design: Techniques to improve energy efficiency," IEEE Solid State Circuits Mag., vol. 7, no. 2, pp. 49–57, Jun. 2015.
[6]. M. Alioto, "Ultra-low power VLSI circuit design demystified and explained: A tutorial," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 1, pp. 3–29, Jan. 2012.
[7]. V. De, S. Vangal, and R. Krishnamurthy, "Near threshold voltage (NTV) computing: Computing in the dark silicon era," IEEE Design Test, vol. 34, no. 2, pp. 24–30, Apr. 2017.
[8]. V. Stojanovic and V. Oklobdzija, "Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems," IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 536–548, Apr. 1999.
[9]. M. Alioto, E. Consoli, and G. Palumbo, "Variations in nanometer CMOS flip-flops: Part I—Impact of process variations on timing," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 62, no. 8, pp. 2035–2043, Aug. 2015.
[10]. Y. Suzuki, K. Odagawa, and M. Hirasawa, "Clocked CMOS calculator circuitry," IEEE J. Solid-State Circuits, vol. SSC-8, no. 6, pp. 462–469, Dec. 1973.
[11]. G. Gerosa et al., "A 2.2 W, 80 MHz superscalar RISC microprocessor," IEEE J. Solid-State Circuits, vol. 29, no. 12, pp. 1440–1454, Dec. 1994.
[12]. Y. Kim et al., "27.8 A static contention-free single-phase-clocked 24T lip-flop in 45 nm for low-power applications," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2014, pp. 466–467.
[13]. Y. Cai, A. Savanth, P. Prabhat, J. Myers, A. S. Weddell, and T. J. Kazmierski, "Ultra-low power 18-transistor fully static contention free single-phase clocked flip-flop in 65-nm CMOS," IEEE J. Solid-State Circuits, vol. 54, no. 2, pp. 550–559, Feb. 2019.
[14]. N. Kawai et al., "A fully static topologically-compressed 21-transistor flip-flop with 75% power saving," in Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC), Singapore, Nov. 2013, pp. 117–120.
[15]. N. Kawai et al., "A fully static topologically-compressed 21-transistor flip-flop with 75% power saving," IEEE J. Solid-State Circuits, vol. 49,no. 11, pp. 2526–2533, Nov. 2014.
[16]. C.-K. Teh et al., "A 77% energy-saving 22-transistor single-phase clock ing D-flip-flop with adaptive-coupling configuration in 40 nm CMOS," in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2011, pp. 338–339.
[17]. V. Loi Le, J. Li, A. Chang, and T. T. Kim, "An 82% energy-saving change-sensing flip-flop in 40 nm CMOS for ultra-low power applications," in Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC), Nov. 2017, pp. 197–200.
[18]. V. L. Le, J. Li, A. Chang, and T. T.-H. Kim, "A 0.4-V, 0.138 fJ/cycle single-phase-clocking redundant-transition-free 24T flip-flop with change-sensing scheme in 40-nm CMOS," IEEE J. Solid-State Circuits, vol. 53, no. 10, pp. 2806–2817, Oct. 2018.
[19]. G. Shin, E. Lee, J. Lee, Y. Lee, and Y. Lee, "An ultra-low-power fully static contention-free flip-flop with complete redundant clock transition and transistor elimination," IEEE J. Solid-State Circuits, vol. 56, no. 10, pp. 3039–3048, Oct. 2021, doi: 10.1109/JSSC.2021.3077074.
[20]. G. Shin et al., "Static contention-free differential flip-flop in 28 nm for low-voltage, low-power applications," in Proc. IEEE Custom Integr. Circuits Conf. (CICC), Mar. 2020, pp. 1–4 .