

High Performance RSP-14TSRAM Cell Design Using 65nm CMOS Technology for Low Power Aerial Applications

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Abstract- Transistor size decreases with technological advances and increases speed. This reduction leads to SRAM cells used for air and space applications. It is vulnerable to radiation, triggering multi-node agitation as well. There are energy-efficient dual node upsets in this article. For low-performance air and space applications, recoverable 14T-SRAM cells were used. In this extend, the modern RSP-14T-SRAM-Bitzelle (radiation remedy in speed and execution) points to make strides speed, execution productivity and unwavering quality in radiation-prone situations. The proposed RSP-14T 8-bit SRAM cell plan by optimizing at the format level of 65 nm-CMOS innovation. By stacking the cooperation impact into the off-state transistor, this plan makes strides flexibility against single occasion disarray and occasions for a few grades of disarray. In high-rating situations, overwhelming particle strikes can ionize semiconductor materials and make intemperate loads that can be recorded at delicate circuit hubs. This makes the placement ideal for radiation curing capabilities.

Keywords: 14T SRAM, Aerospace Applications, Tanner EDA, High-Performance Memory and 65 nm CMOS.

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I. INTRODUCTION

The process of creating coordinate circuits by assembling thousands of transistor circuits onto a single chip is known as SY-Large Scale Integration, or VLSI. VLSI stands for "Exceptionally Large Grid." The Gadgets industry has achieved great developments over the past 20 years, particularly with the rapid advances in integrated innovation, the advent of large-scale framework plans - VLSI. The number of coordinate circuit applications in high-performance computing, wireless communications and buyer hardware has risen relentlessly at a very fast pace.

As demand for low-performance high-speed electronic systems proceeds, memory components have emerged as a key area for optimization. Due to quick access times and low latency, SRAM is often used in microprocessors, cache memory and portable devices. Traditional SRAM designs, particularly 6T cell 6 transistors (6T), have served as industry standard for decades. With advances in technology scaling and ultra-low power systems, improvements in SRAM architecture have become necessary to overcome challenges related to stability, leakage and variation [26].

This design shows the following great features: 1) EDP14T EXHIBS eliminates complete immunity to two polarities. This is directed against any sensitive knot. 2) As most comparative cells during the reading process, consume a small amount of energy during writing and decreasing energy. 3) The suggested cells consume less performance than the majority of cells taken into consideration. 4) EDP14T has higher writing capabilities and short writing delays than many comparison cells [1].

➤ *The 12T SRAM Cell has Some Drawbacks Despite Being an Improvement Over the Conventional 6T Architecture, Including:*

- Moderate noise margins under aggressive voltage scaling;
- Power inefficiencies during switching events; and
- Possible reliability issues at deep sub-micron technologies.

By increasing read/write stability, reducing soft mistakes, and boosting noise immunity, the proposed 14T SRAM cell seeks to address these problems while preserving a competitive latency and power profile. The suggested 14T

SRAM cell is thus a development of the 12T concept. Two more transistors, PMOS and NMOS, are added and connected to the QB node. These transistors enhance immunity to noise and charge sharing while reinforcing logic levels during data preservation. This results in:

- Static noise margin (SNM) enhancement
- A decreased likelihood of soft errors
- An Improved data preservation in the face of voltage variations

➤ *The Following Crucial Performance Metrics Were Assessed in This Study:*

- Average Power Consumption: Shows the cell's energy efficiency.
- Power Maximum and Minimum: Crucial for thermal design.
- The speed of read/write operations is measured by the propagation delay.
- Static Noise Margin: Indicates data integrity and stability.

The following describes how this paper is presented. The literature evaluation of earlier efforts is covered in Section III, the operation and constraints of the current 12T SRAM design were explained. The design of the suggested 14 T SRAM cell is covered in Section IV. Section V discusses the simulation setup and comparison.

II. LITERATURE SURVEY

The EDP12T SRAM cell, proposed by S. Pal et al. (2023), is totally immune to SEUs that occur at all of its sensitive nodes. Additionally, SEMNUs placed at its innermost pair of nodes cause EDP12T to fully recover. Compared to most of the cells considered, EDP12T has a shorter TWA and a higher write ability. As a result, EDP12T is an excellent material for use in aircraft [1].

A radiation-hardened SRAM cell designed for space use with reduced power was presented by S. Pal et al. in 2021. In this paper, Soumitra Pal, D. D. Sri, W.-H. Ki, and A. Islam focus on Single Event Upsets (SEUs), which are common in space environments. The SRAM cell's resistance to radiation degradation guarantees data integrity in demanding space settings [2].

According to S. Pal et al. (2021), suggested a Soft- error-immune read stability-improved SRAM for multi- node upset tolerance in space applications with best-read stability obtained by memory cells in deep sub-micron technique [3].

The SARP12T, a 12-transistor (12T) SRAM cell designed for aerospace applications to lessen radiation-induced soft errors, is described by S. Pal et al. (2022). According to ijarcce.com, this cell can recover from SEU and SEMNU, and it also enhances read stability. This is achieved by ensuring data recovery even if sensitive nodes are flipped by radiation [4].

Jiang J. et al. (2019), This study suggests quadruple cross-coupled storage cells (QUCCE) in 130nm CMOS technology with capacities of 10T and 12T. Additionally, compared to most referential cells, including the 6T, the QUCCE 12T saves more than 50% on read access time. It is hence suitable for high-speed SRAM designs. Consequently, the QUCCE 12T is a viable choice for future reliable terrestrial low-voltage applications [5].

A soft error tolerant SRAM cell with quad-node ten transistors (10 T) that offers differential read operation for dependable sensing was proposed by S. M. Jahinuzzaman et al. (2009). The recommended cell significantly reduces leakage power by providing a noise margin. Using a 32-kb SRAM integrated into 90-nm CMOS technology, the cell also shows a 98% lower soft error rate than the 6 T cell in TRIUMF's accelerated neutron radiation studies [6].

SRAM cells, used in space, are particularly susceptible to soft-error, according to S. Pal et al. (2021). The most proficient writer is RHRD12T. In terms of write delay, RHRD12T performs better. Additionally, of all the comparison cells, RHRD12T can tolerate the greatest critical charge and is the least susceptible to single-event disturbances. The benefits mentioned above come at the cost of longer read delay [7].

L. D. T. Dang et al. (2017) presented the we- Quatro, a 12T SRAM cell. The suggested SRAM cell takes up roughly the same amount of area as Quatro, despite utilizing more transistors. Our comprehensive simulations validate the effectiveness of our suggested we-Quatro, demonstrating that the suggested cell offers comparable soft-error resilience and good writability to Quatro under with other radiation-hardened SRAM cells. Finally, Section VI concludes the article. parametric variations of 28-nm fully depleted SOI technology [8].

C. Qi, L. Xiao, and others (2016), A very reliable memory cell (RHD12) based on a commercial 65-nm CMOS technology with 12 transistors is shown in this study. In addition to fully tolerating single-event upsets that occur on any one of its single nodes. The RHD12 and other cutting-edge memory cells are further assessed using a number of HSPICE post-simulations, which demonstrate that our suggested memory cell outperforms the others in terms of area, power consumption, and access time [9].

C. Peng and associates (2019), A radiation- hardened 14T SRAM bit cell with a high power and speed rating for space applications. This bit cell, called the RSP- 14T, is designed to perform better than the RHD-12T by offering better radiation tolerance, speed, and power consumption. The RSP-14T uses a source isolation approach and circuit and layout optimization to achieve these gains [10].

S. Pal et al. (2021) For space applications, recommend a 10T Soft-Error-Immune SRAM. SIS10T is compared to QUATRO10T, QUATRO12T, QUCCE12T, DICE12T, and RHD12T in order to determine its relative performance. SIS10T can recover from single-event multi- node upsets at

its internal node-pair as well as single-event upsets of both polarities caused at all sensitive nodes [11].

S. Pal et al. (2022) A 10T Soft-Error-Immune SRAM was suggested for use in space applications. SIS10T is compared to QUATRO10T, QUATRO12T, QUCCE12T, DICE12T, and RHD12T in order to determine its relative performance. All sensitive nodes experienced both single-event disturbances of both polarities, and single-event multi-node upsets at its internal node-pair can be recovered from using SIS10T [12].

J. Guo et al. (2014) proposed a revolutionary low- power and highly reliable radiation-hardened memory cell with 12 transistors using TSMC 65 nm CMOS technology. The obtained results demonstrate that, regardless of the polarity and strength of the upset, the suggested cell can withstand it at any sensitive node, and can recover from multiple-node upset generated by charge sharing on the fixed nodes, regardless of the stored value. Furthermore, the proposed cell has overheads of static power, area, and access time that are the same or lower than previous radiation-hardened memory cells [13].

Q. Zhao et al (2020), discussed "Very dependable and novel write-enhanced RHPD-12T SRAM cells for space applications." This cell design aims to improve SRAM write speed and reliability for use in challenging environments, including space, where radiation mistakes could occur. It is highlighted that it is more stable and has a lower write delay than other 12T SRAM cells [14].

Soft errors like MNU and SNU have a key problem for SRAMs in both terrestrial and airborne applications, according to G. Prasad et al. (2021). The observed findings determine the LWS14T can recover from both SNUs and MNUs, irrespective of the upset polarity. Additionally, compared to similar RHBD cells. The LWS14T delivers lower power and delay costs. Furthermore, the LWS14T offers enhanced critical charge, stability, and writability [15].

According to A. Yan et al. (2020), as CMOS technology continue to advance, SRAMs are becoming more prone to soft errors. This paper presents S4P8N and S8P4N, two new radiation-hardened SRAM cell designs with enhanced self-recoverability from SNU DNUs. It was proposed to use the S4P8N cell with redundant nodes and additional access transistors [16–19].

III. EXISTING METHOD

SRAM is an essential aspect of digital systems, especially in high-reliability and aerospace applications where radiation tolerance is crucial. The 12T SRAM cell is unique among SRAM architectures because it strikes a balance between speed, power consumption, and soft-error tolerance. This chapter offers a thorough examination of the traditional 12 Transistor SRAM design, going over its merits, functioning, circuit architecture, and inherent drawbacks that drive the need for a more reliable 14T architecture. The 12T SRAM cell is composed of 6 transistors that produce two cross- coupled inverters, just like a conventional 6T, plus extra transistors to improve radiation robustness and read/write decoupling as shown in Fig. 1 and its circuit design using Tanner tool is depicted in Fig. 2 [20-25].

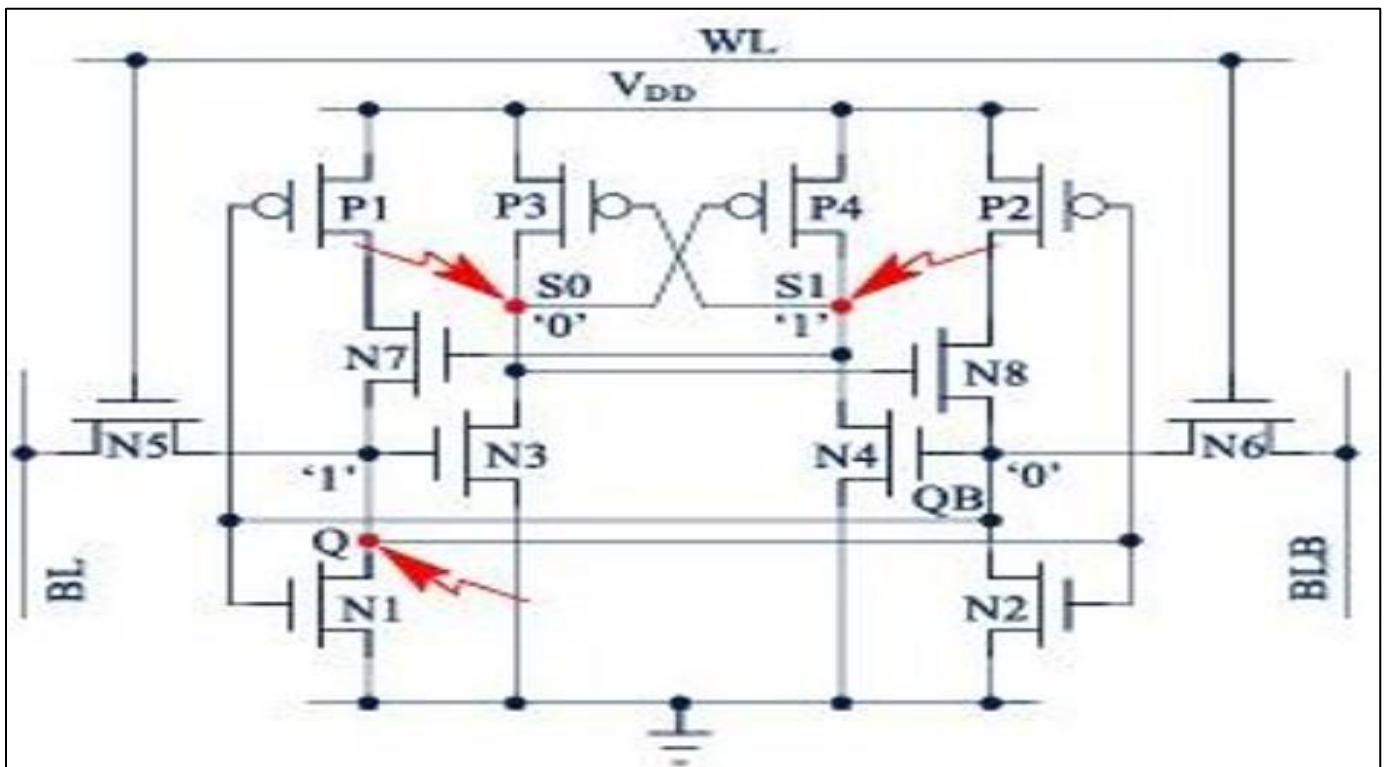


Fig. 1. Existing Method 12T SRAM Circuit

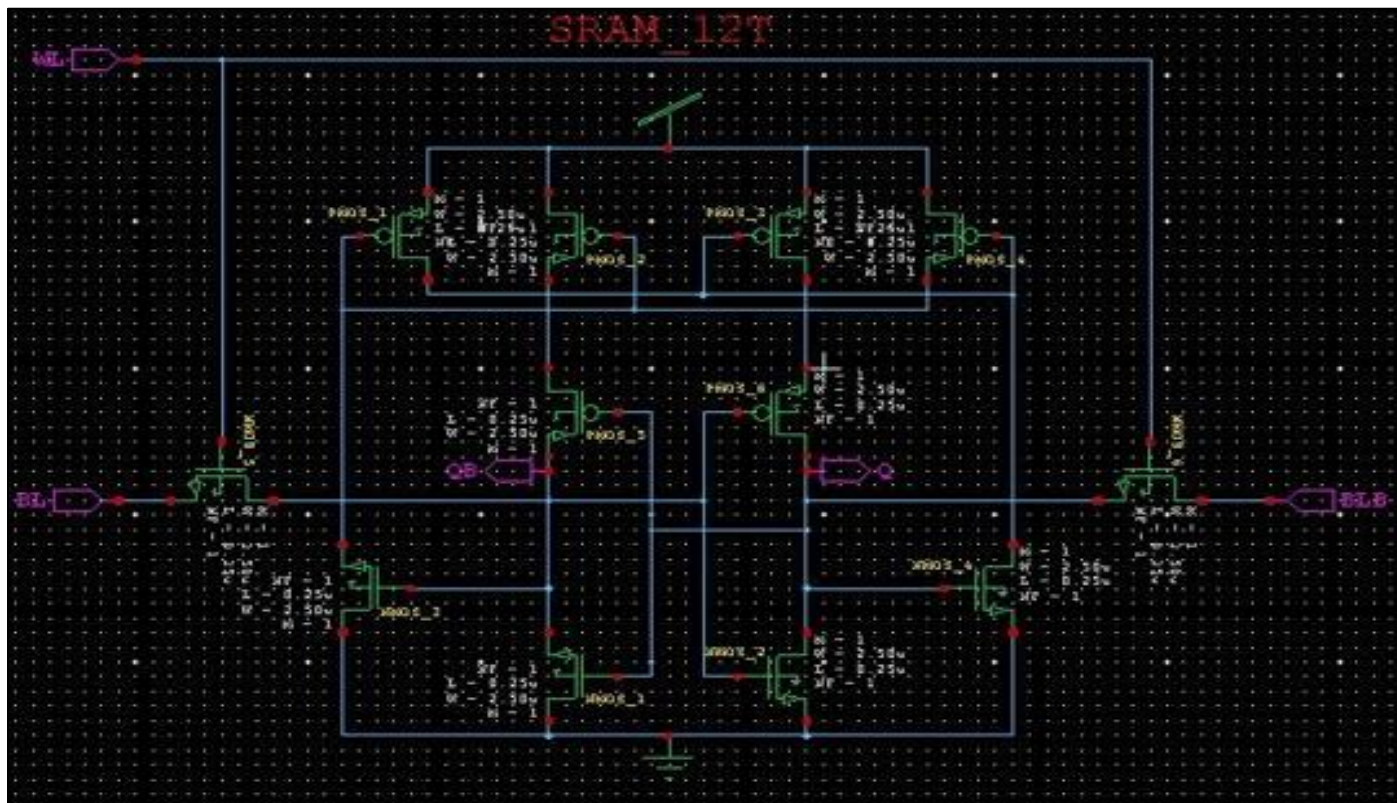


Fig 2 Existing Method 12T SRAM Circuit Design Using Tanner Tool

➤ *Limitations of 12T SRAM Cell:*

The 12T SRAM cell has many drawbacks in spite of its benefits:

• *Area Overhead:*

For high-density memory arrays, additional transistors result in a much larger layout area, which reduces efficiency.

• *Power Consumption:*

Higher dynamic and leakage power are the results of

more transistors and independent control lines.

• *Write Latency:*

Because write access transistors are weaker than storage inverters, write performance may be impacted even though write latency is steady [24-28].

The comparison of various SRAM cells with different parameters were illustrated in Table. 1

Table 1 Comparison of different parameters with SRAM cells

Parameter	SRAM Cells		
	6T	10T	12T
Stability(Read)	Small	Medium	Large
Stability(Write)	Large	Large	Medium
Area Effectiveness	Large	Medium	Small
Utilization of Power	Small	Medium	Large
SEU Tolerance	Low	Moderate	High
Delay	Low	Moderate	High
Cost	Low	Moderate	High

IV. PROPOSED METHOD

The proposed 14-transistor (14T) SRAM cell is to improve overall dependability, data stability, and radiation immunity in hostile settings like space and aerospace missions. The necessity to address the drawbacks of traditional 12T designs, especially in improved write margin, area optimization, and multi-node upset tolerance in situations involving ionizing radiation, served as the primary driving force behind the design of the 14T cell. A memory-

by- design (MbD) technique was used in the creation of the 14T cell, it has additional transistors to carefully isolate the storage nodes from the read and write functions.

By combining read and write decoupling with dual-port access, the suggested design enhances soft error resistance and lowers the chance of data corruption during concurrent operations. This improvement maintains low power usage while greatly enhancing multiple-node upset (MNU) and single-event upset (SEU) immunity. Additionally, Tanner

EDA 16.3 with post-layout analysis is used to simulate and test the suggested cell in order to guarantee its viability for practical implementation in contemporary CMOS

technologies. Fig. 3 shows the circuit architecture of the suggested 14T SRAM cell and its circuit design using Tanner tool is also illustrated in Fig. 4.

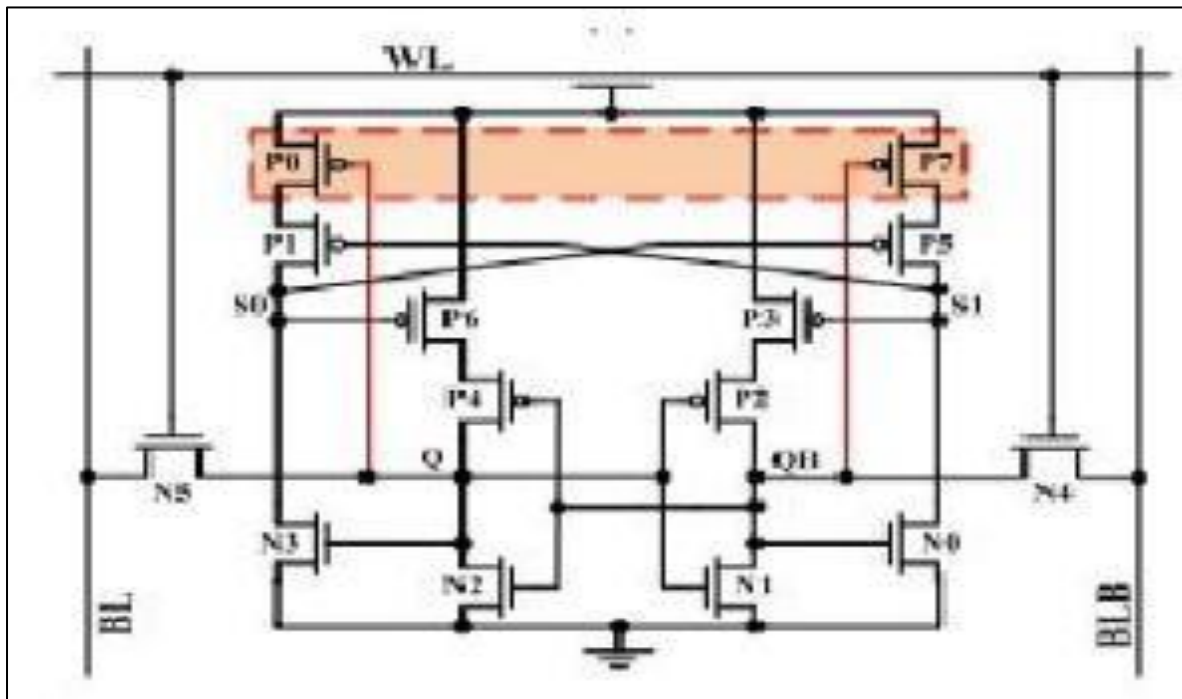


Fig 3 14T SRAM Cell Circuit

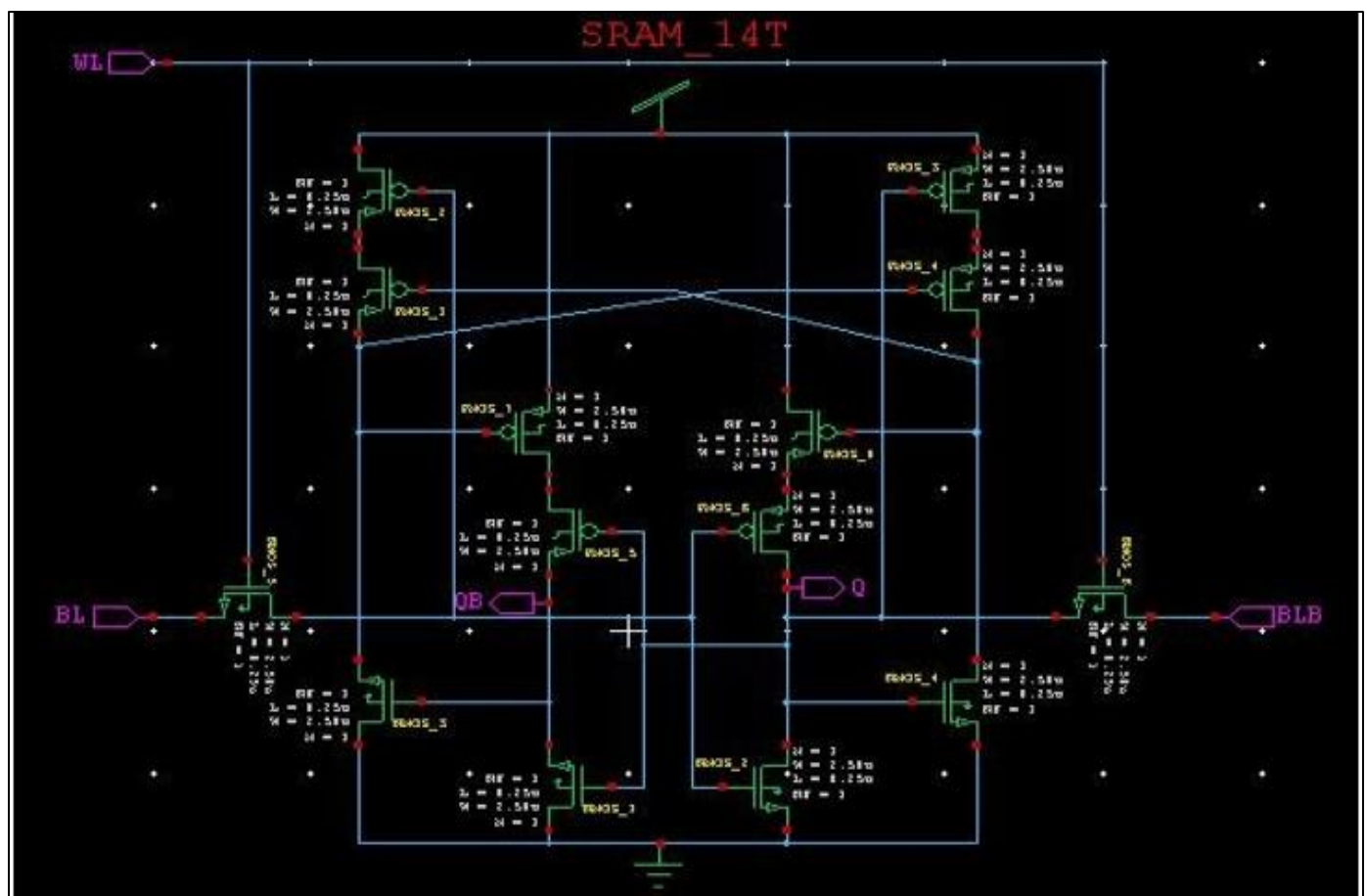


Fig 4 14T SRAM Cell Circuit Design Using Tanner Tool

V. RESULTS AND DISCUSSIONS

The 12 T and 14 T SRAM cell simulation results, with an emphasis on power consumption and latency are shown in below figures respectively using Tanner tool.

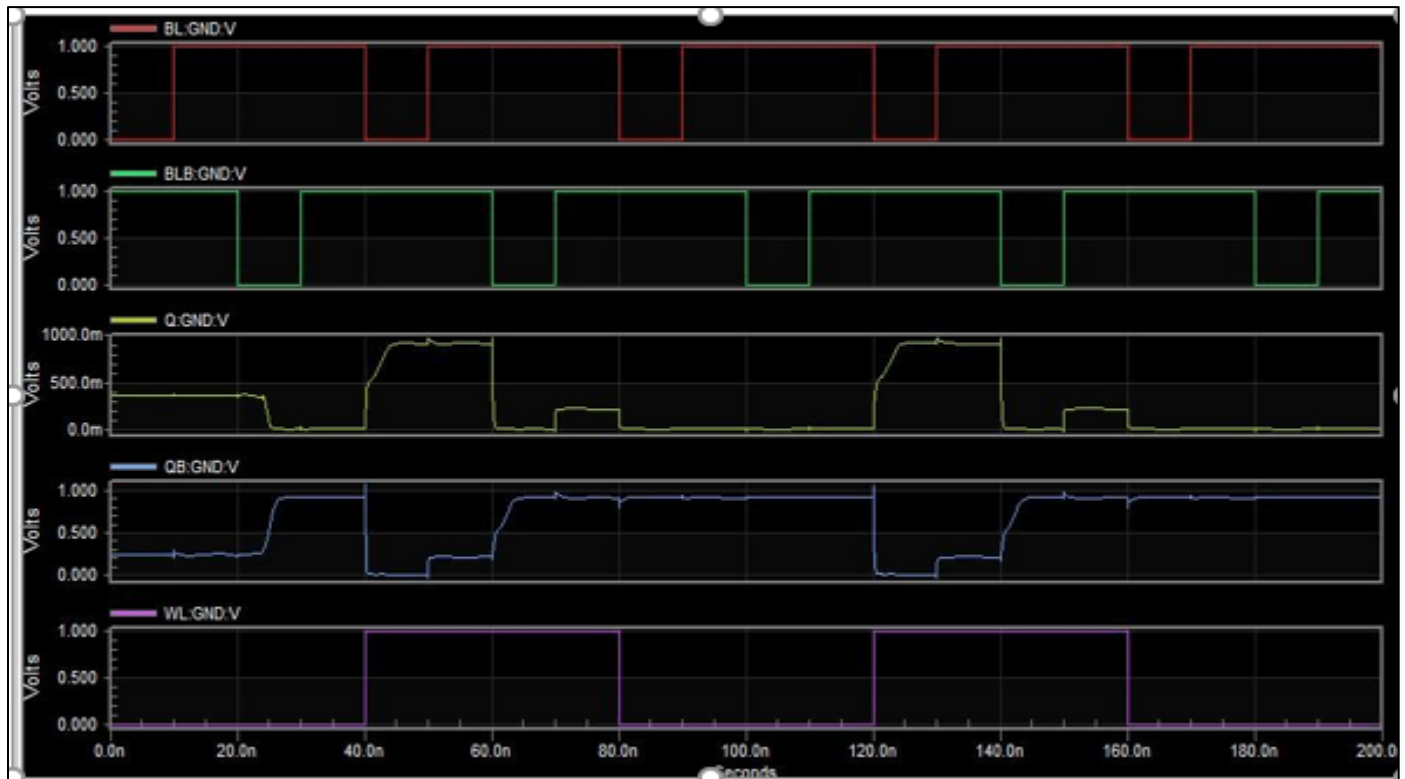


Fig 5 Simulation Result for 12T SRAM Cell Design

Fig 5 Shows the timing diagram, which makes it easier to see how the 12T SRAM cell behaves dynamically and shows how data is written and stored inside the cell. Similar to the findings we saw for the 12T cell.

➤ Power Performance:

• VDD between 0 to 2e-007:

This shows that the simulation ran for 200 nanoseconds, or 2×10^{-7} seconds.

• Average Power Consumed -> 2.177112e-005 watts:

This represents the 12T SRAM cell's average power dissipation during the course of the simulation. This

amounts to 21.77 microwatts, or 0.00002177112 watts, in decimal units.

• Maximum Power 1.266422e-001 at Time 1.6e-007:

At 160 nanoseconds into the simulation, the highest power use in real time was 0.1266422 watts (126.6 milliwatts).

• Minimum Power 7.638291e-006 at Time 1.9e-007:

At 190 nanoseconds, the minimal power use in real time was 0.000007638291 watts (7.638 microwatts).

➤ 12T Power Efficiency & Delay:

```
Power Results

VDD from time 0 to 2e-007
Average power consumed -> 2.177112e-005 watts
Max power 1.266422e-001 at time 1.6e-007
Min power 7.638291e-006 at time 1.9e-007

Measure information will be written to file "D:\tanner\SRAM_DESIGN_AE

Measurement result summary
delay1      = 20.1202n
delay2      = 50.1202n
delay3      = 30.1202n
```

➤ *Measurement Delays:*• *Delay1 = 20.1202n:*

A delay of 20.1202 nanoseconds is indicated by this value. The amount of time a signal takes to get from the bit line to the storage node or from the word line to the bit line is probably a reference to a particular transition period inside the cell.

• *Delay2 = 50.1202n:*

This is an additional 50.1202 nanosecond delay measurement. It could signify a distinct change or a more intricate process with several steps.

• *Delay3 = 30.1202n:*

This is a third measurement of the delay, which is 30.1202 nanoseconds. It can be an additional property of the cell's latency.

➤ *Summary:*• *Power Efficiency:*

The 12T SRAM cell has a respectable power efficiency, as seen by its average power usage of 21.77 microwatts. The much greater peak power usage indicates that switching events play a significant role in power dissipation.

• *Delay:*

The cell's speed can be inferred from the delay numbers (20.1202ns, 50.1202ns, and 30.1202ns). The entire performance of the memory is directly impacted by these delays, which dictate how fast the cell may be written to or read from. Different critical routes within the cell are probably represented by the various delay values.

Fig 6 shows the simulation results for the 14T SRAM cell, with an emphasis on power consumption and latency.

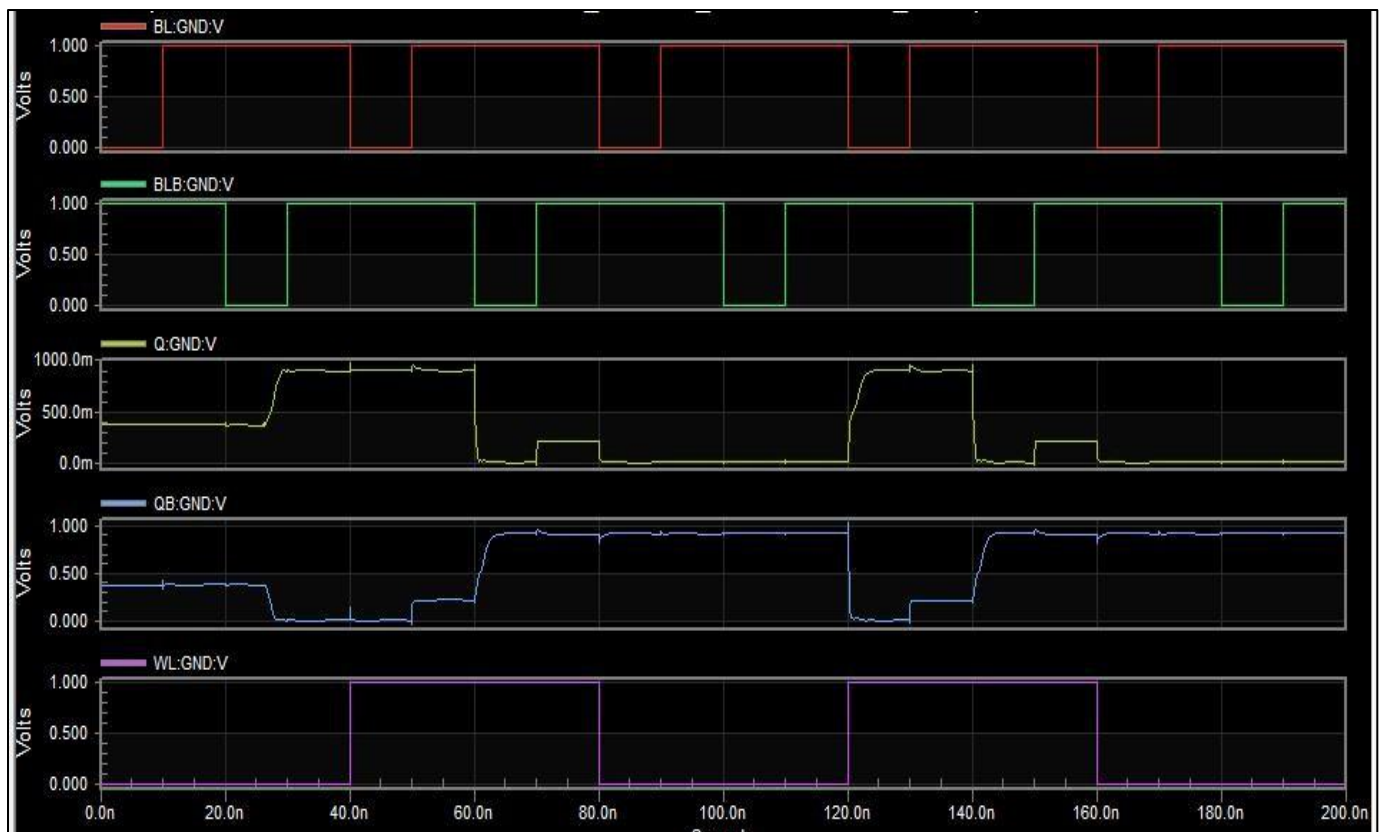


Fig 6 Simulation Result for 14T SRAM Cell Design

➤ *Power Performance:*• *VDD Between 0 and 2e-007:*

This shows that the simulation ran for the same amount of time as the 12T simulation, or 2×10^{-7} seconds (200 nanoseconds).

• *Average Power Consumed -> 2.572317e-005 watts:*

This represents the 14T SRAM cell's average power dissipation during the simulation. This is equivalent to 0.00002572317 watts, or 25.72 microwatts, in decimal units.

• *Maximum Power 1.740072e-001 at Time 8e-008:*

At 80 nanoseconds into the experiment, the highest power use in real time was 0.1740072 watts, or 174 milliwatts.

• *Minimum Power 8.904335e-006 at Time 1.90019e-007:*

The lowest instantaneous power consumption at 190.019 nanoseconds was 0.000008904335 watts (8.90 microwatts).

➤ *14T Power Efficiency & Delay:*

```
Power Results

VDD from time 0 to 2e-007
Average power consumed -> 2.572317e-005 watts
Max power 1.740072e-001 at time 8e-008
Min power 8.904335e-006 at time 1.90019e-007

Measure information will be written to file "D:\tanner\

Measurement result summary
delay1          = 20.1372n
delay2          = 50.1372n
delay3          = 30.1372n
```

➤ *Measurement Delays:*

- *Delay1 = 20.1372n:*
This denotes a 20.1372 Nano second delay.
- *Delay2 = 50.1372n:*
This is an additional delay measurement of 50.1372 nano seconds.
- *Delay3 = 30.1372n:*
This is a third delay measurement of 30.1372 nano seconds.

➤ *Comparison of 14T with 12T SRAM Cells:*

Let's contrast these findings with the 12T SRAM data to gain a better understanding:

- *Average Power:*
The average power consumption of the 14T cell is slightly greater at 25.72 microwatts than that of the 12T cell,

which is 21.77 microwatts. Because the 14T architecture has more transistors, this is to be expected.

- *Maximum Power:*
In addition, the 14T cell uses more power at its maximum (174 milliwatts) than the 12T cell (126.6 milliwatts).
- *Minimum Power:*
The minimum power of the 14T cell is 8.90 microwatts, which is slightly higher than that of the 12T cell (7.638 microwatts).
- *Delays:*
The 14T cell's delay values (20.1372ns, 50.1372ns, and 30.1372ns) are nearly identical to the 12T cell's, but marginally higher (20.1202ns, 50.1202ns, and 30.1202ns). The comparison of 14T with 12T SRAM cell is illustrated in Table. 2 in terms of power and delay.

Table 2 Comparison of Different Parameters with SRAM Cells

Parameter	SRAM Cells	
	12T	14T
Average Power	21.77 μ W	25.72 μ W
Maximum Power	126.6 mW	174 mW
Minimum Power	7.638 μ W	8.90 μ W
Delay 1	20.1202 ns	20.1372 ns
Delay 2	50.1202 ns	50.1372 ns
Delay 3	30.1202 ns	30.1372 ns

In above, compared to the 12T SRAM cell, the 14T SRAM cell provides better stability at the expense of somewhat larger delays and slightly higher power consumption. The power consumption characteristics of 12T and 14T SRAM cells are contrasted in the following bar graph (Fig. 7.).

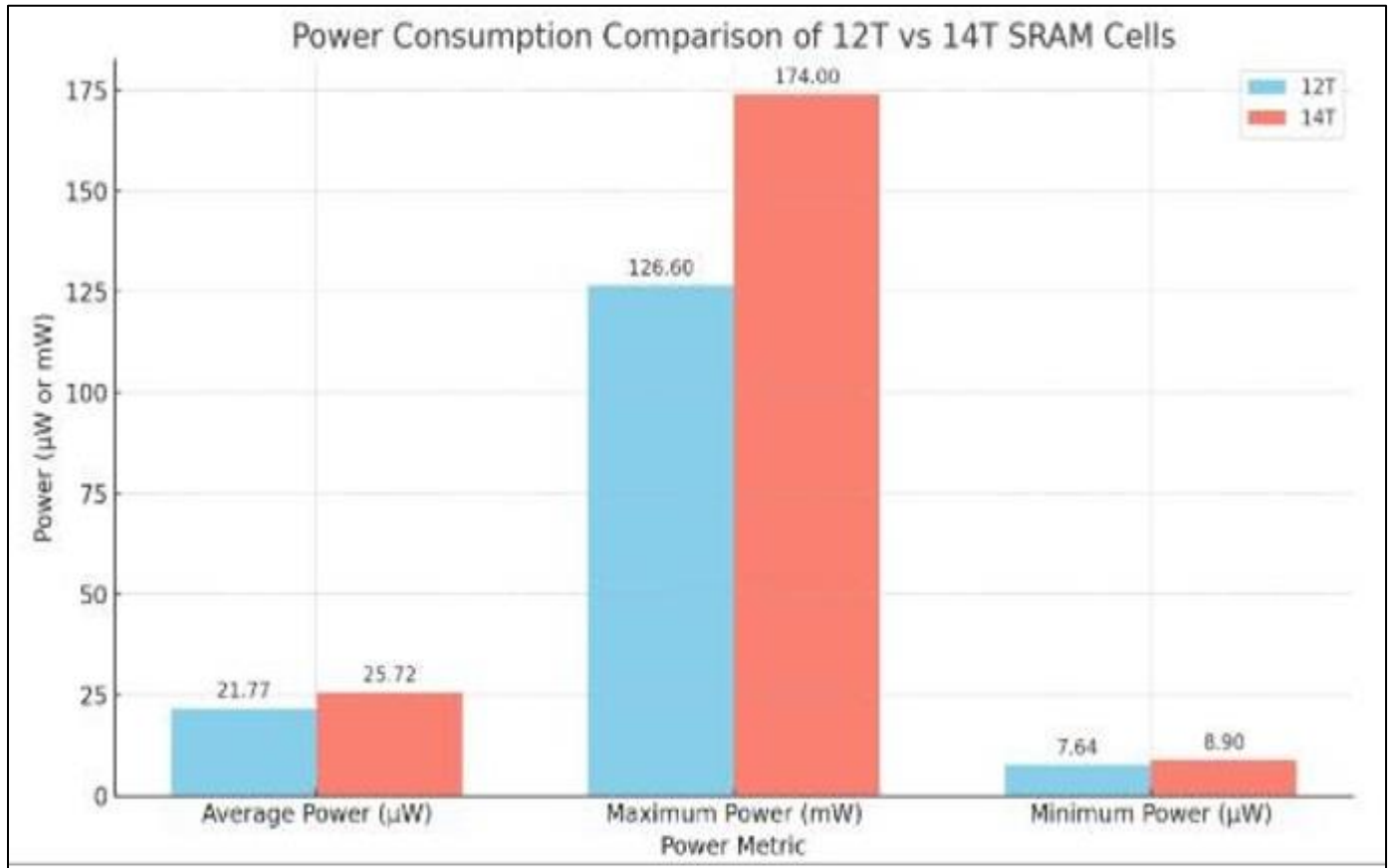


Fig 7 Power Consumption Comparison

The following bar graph (Fig. 8) compares the delay characteristics of 12T and 14T SRAM cells:

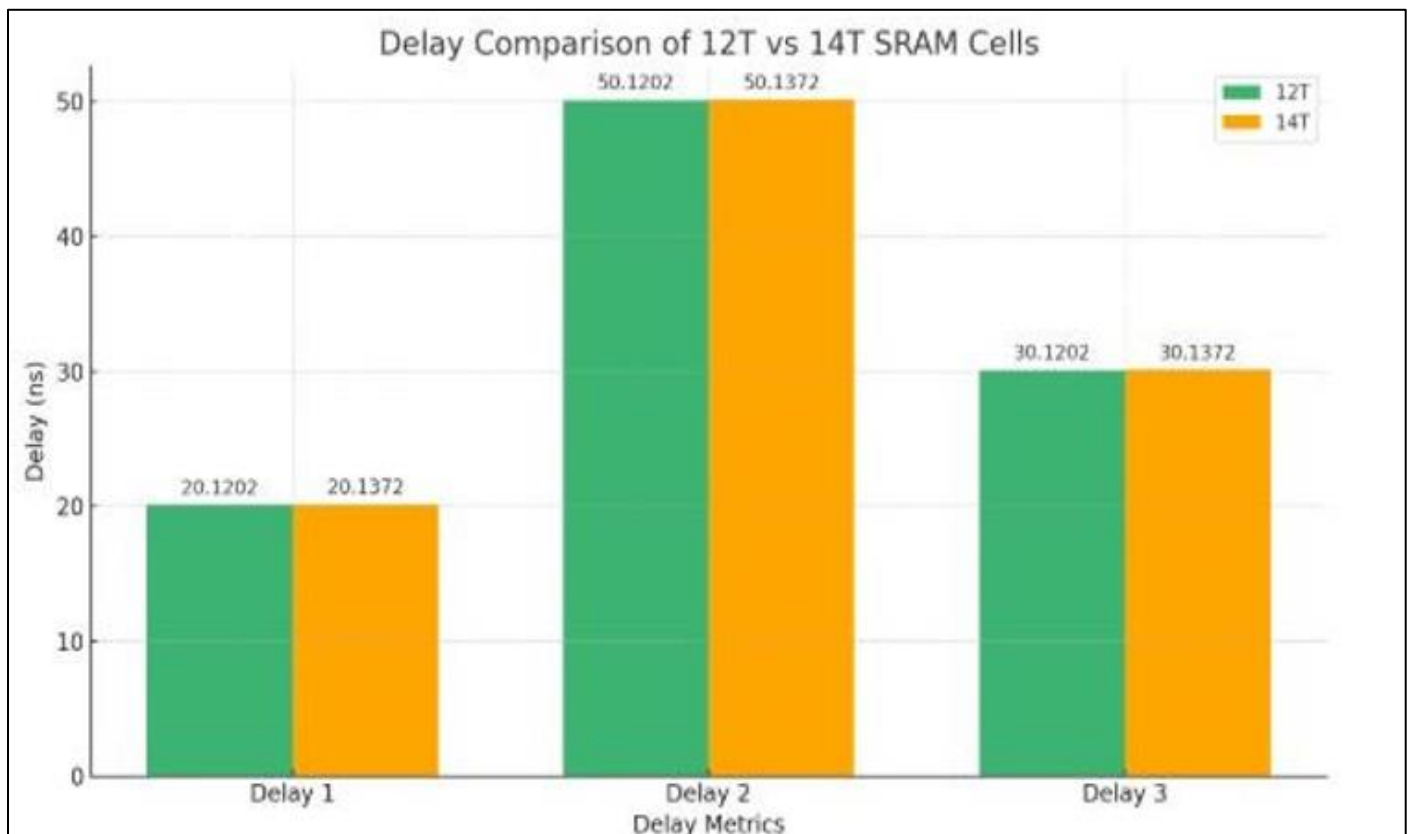


Fig 8 Delay Comparison

VI. CONCLUSION AND FUTURE SCOPE

In this design, a unique applications requiring radiation resistance and soft error immunity can benefit from the 14T SRAM cell architecture. was thoroughly designed, simulated, and compared. The shortcomings of traditional 12T SRAM designs, namely with regard to multi-node upset tolerance, soft error susceptibility, and data stability in demanding settings like space and aerospace missions, were addressed by the proposed 14T SRAM cell. The 14T cell produced significant increases in write ability, soft error resilience, and static noise margin (SNM) by improvements in feedback mechanisms, layout-level optimizations, and distinct read/write access pathways, among other circuit- level advances. The suggested cell performed better under a variety of operational situations, such as changes in voltage and temperature, according to extensive simulations conducted with Tanner EDA 16.3. Given its resilience and dependability, compared to the 12T design, the 14T cell's little increase in area and power consumption is well worth the trade-off. These outcomes confirm that the 14T SRAM cell is a viable option for embedded systems that are susceptible to radiation.

Although the suggested 14T SRAM design provides notable gains in data stability and radiation tolerance, more can be done to increase its suitability for use in upcoming nanoscale CMOS technologies. Optimizing the 14T architecture for cutting-edge technological nodes like 28nm is one encouraging avenue.

REFERENCES

- [1]. S. Pal, G. Chowdary, W. -H. Ki and C. -Y. Tsui, "Energy- Efficient Dual-Node-Upset-Recoverable 12T SRAM for Low- Power Aerospace Applications," in *IEEE Access*, vol. 11, pp. 20184-20195, 2023, doi:10.1109/ACCESS.2022.3161147.
- [2]. S. Pal, D. D. Sri, W.-H. Ki, and A. Islam, highly stable low power radiation hardened memory-by-design SRAM for space applications, *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 6, pp 2147-2151, Jun. 2021, doi: 10.1109/TCSII.2020.3042520.
- [3]. S. Pal, S. Mohapatra, W.-H. Ki, and A. Islam, Soft-error- immune read stability-improved SRAM for multi-node upset tolerance in space applications, *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 8, pp. 33173327, Aug. 2021, doi: 10.1109/TCSI.2021.3085516.
- [4]. S.Pal,W.-H. Ki, and C.-Y.Tsui, Soft-error-aware read-stability- enhanced low-power 12T SRAM with multi-node upset recoverability for aerospace applications, *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 4, pp. 15601570, Apr. 2022, doi: 10.1109/TCSI.2022.3147675..
- [5]. J. Jiang, Y. Xu, W. Zhu, J. Xiao, and S. Zou, Quadruple cross- coupled latch-based 10T and 12T SRAM bit-cell designs for highly reliable terres trial applications, *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 3, pp. 967977, Mar. 2019, doi: 10.1109/TCSI.2018.2872507.
- [6]. S. M. Jahinuzzaman, D. J. Rennie, and M. Sachdev, A soft error tolerant 10T SRAM bit-cell with differential read capability, *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 37683773, Dec. 2009, doi: 10.1109/TNS.2009.2032090.
- [7]. S. Pal, D. Divya, W. Ki, and A. Islam, Radiation-hardened read decoupled low-power 12T SRAM for space applications, *Int. J. Circuit Theory Appl.*, vol. 49, no. 11, pp. 35833596, Nov. 2021. [Online]. Available:<https://onlinelibrary.wiley.com/doi/abs/10.1002/cta.3093>
- [8]. L. D. T. Dang, J. S. Kim, and I. J. Chang, We-quatro: Radiation hardened SRAM cell with parametric process variation tolerance, *IEEE Trans. Nucl. Sci.*, vol. 64, no. 9, pp. 24892496, Sep. 2017, doi: 10.1109/TNS.2017.2728180.
- [9]. C. Qi, L. Xiao, T. Wang, J. Li, and L. Li, A highly reliable memory cell design combined with layout-level approach to tolerant single-event upsets, *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 3, pp. 388395, Sep. 2016, doi: 10.1109/TDMR.2016.2593590.
- [10]. C. Peng, Radiation-hardened 14T SRAM bit cell with speed and power optimized for space application, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 2, pp. 407415, Nov. 2019, doi: 10.1109/TVLSI.2018.2879341.
- [11]. S. Pal, S. Sahay, W.-H. Ki, and C.-Y. Tsui, A 10T soft-error- immune SRAM with multi-node upset recovery for low-power space applications, *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 6, pp. 24702480, Jun. 2021, doi: 10.1109/TCSI.2021.3064870.
- [12]. S. Pal, S. Sahay, W. -H. Ki and C. -Y. Tsui, "A 10T Soft-Error- Immune SRAM With Multi-Node Upset Recovery for Low- Power Space Applications," in *IEEE Transactions on Device and Materials Reliability*, vol. 22, no. 1, pp. 85-88, March 2022, doi: 10.1109/TDMR.2022.3147864
- [13]. J. Guo, L. Xiao, and Z. Mao, Novel low-power and highly reliable radiation hardened memory cell for 65 nm CMOS technology, *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 7, pp. 19942001, Jul. 2014, doi: 10.1109/TCSI.2014.2304658.
- [14]. Q. Zhao, C. Peng, J. Chen, Z. Lin, and X. Wu, Novel write- enhanced and highly reliable RHPD-12T SRAM cells for space applications, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 28, no. 3, pp. 848852, Mar. 2020, doi: 10.1109/TVLSI.2019.2955865.
- [15]. G. Prasad, B. C. Mandi, and M. Ali, Soft-error-aware SRAM for terrestrial applications, *IEEE Trans. Device Mater. Rel.*, vol. 21, no.4, pp. 658660, Dec.2021,doi:10.1109/TDMR.2021.3118715.
- [16]. A. Yan, Y. Chen, Y. Hu, J. Zhou, T. Ni, J. Cui, P. Girard, and X. Wen, Novel speed-and-power-optimized sram cell designs with enhanced self-recoverability from single- and double-node upsets, *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12,pp. 46844695, 2020, doi: 10.1109/TCSI.2020.3018328

- [17]. A. Yan, Z. Wu, J. Guo, J. Song, and X. Wen, Novel double- node-upset tolerant memory cell designs through radiation- hardening-by-design and layout, *IEEE Trans. Rel.*, vol. 68, no. 1, pp. 354363, Mar. 2019, doi: 10.1109/TR.2018.2876243.
- [18]. A. Yan, Z. Xu, X. Feng, J. Cui, Z. Chen, T. Ni, Z. Huang, P. Girard, and X. Wen, Novel quadruple-node-upset-tolerant latch designs with optimized overhead for reliable computing in harsh radiation environments, *IEEE Trans. Emerg. Topics Comput.*, vol. 10, no. 1, pp. 404413, Jan. 2022, doi: 10.1109/TETC.2020.3025584.
- [19]. A. Yan, Y. Hu, J. Cui, Z. Chen, Z. Huang, T. Ni, P. Girard, and X. Wen, Information assurance through redundant design: A novel TNU error resilient latch for harsh radiation environment, *IEEE Trans. Comput.*, vol. 69, no. 6, pp. 789799, Jun. 2020, doi: 10.1109/TC.2020.2966200.
- [20]. M. Moghaddam, M. H. Moaiyeri, and M. Eshghi, Design and evaluation of an efficient Schmitt trigger-based hardened latch in CNTFET technology, *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 1, pp. 267277, Mar. 2017, doi: 10.1109/TDMR.2017.2665780.
- [21]. J. Guo, L. Xiao, T. Wang, S. Liu, X. Wang, and Z. Mao, Soft error hardened memory design for nanoscale complementary metal oxide semiconductor technology, *IEEE Trans. Rel.*, vol. 64, no. 2, pp. 596602, 2015, doi: 10.1109/TR.2015.2410275.
- [22]. J. P. Kulkarni, K. Kim, and K. Roy, A 160 mV robust Schmitt trigger based subthreshold SRAM, *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 23032313, Oct. 2007, doi: 10.1109/JSSC.2007.897148.
- [23]. E. Abbasian, M. Gholipour, Design of a highly stable and robust 10T SRAM cell for low-power portable applications, *Circuits Syst. Signal Process* 41 (10) (2022) 5914–5932, <https://doi.org/10.1007/s00034-022-02054-y>.
- [24]. M. Elangovan, D. Karthickeyan, M. Arul Kumar, R. Ranjith, Darlington based 8T CNTFET SRAM cells with low power and enhanced write stability, *Trans. Electr. Electron. Mater.* (2021), <https://doi.org/10.1007/s42341-021-00329-w>.
- [25]. R. Nematirad, A. Pahwa, B. Natarajan, H. Wu, Optimal sizing of photo voltaic battery system for peak demand reduction using statistical models, *Front. Energy Res.* 11 (2023) 1297356.