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EMI Optimization of a Wi-Fi-Enabled Relay Module for Smart Home Application Using ESP8266/N76E003

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Abstract: **Modern smart home devices integrate wireless communication and power switching functions on compact printed circuit boards (PCBs), making them vulnerable to electromagnetic interference (EMI). This work investigates the optimization of a Wi-Fi-enabled relay module based on the ESP8266 and N76E003 microcontroller. The approach combines finite element modeling in Ansys SIwave with PCB-level design countermeasures. Key optimizations included improved decoupling, via stitching, and stack-up refinement. Simulation and validation results show significant reductions in power distribution network resonances and transient emissions, ensuring compliance with CISPR Class B. The study demonstrates that systematic PCB design improvements effectively enhance the electromagnetic compatibility of IoT modules.**

Keywords*: ***Electromagnetic Interference; Electromagnetic Compatibility; Smart Home IoT; Wi-Fi Module; PCB Optimization; Finite Element Method ; Power Distribution Network.

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I. INTRODUCTION

The exponential growth of the Internet of Things (IoT) transforms residential environments into interconnected smart systems. Devices with wireless communication and remote actuation are now ubiquitous in applications such as home automation, energy management, and security. However, the integration of wireless modules, microcontrollers, and power-switching elements on compact printed circuit boards (PCBs) brings one of the most persistent challenges in modern electronics: electromagnetic interference (EMI). Compliance with international standards such as CISPR 22/32 and FCC Part 15 is mandatory, particularly for consumer devices operating in electromagnetically dense residential environments [2], [3].

Electromagnetic interference arises from multiple coupling mechanisms, including capacitive, inductive, conducted, and radiated paths. As shown in Fig. 1, the studied module integrates several EMI sources: ESP8266 Wi-Fi RF emissions, relay switching transients, and regulator-induced PDN noise. These affect victims such as the N76E003 microcontroller, Wi-Fi signals, and nearby IoT devices. The interactions occur through conductive coupling via supply rails, capacitive coupling between traces, inductive coupling through relay loops, and radiative coupling from PCB traces acting as unintentional antennas. This coexistence of RF, digital, and electromechanical elements makes Wi-Fi-enabled relay modules a challenging case for EMI optimization.

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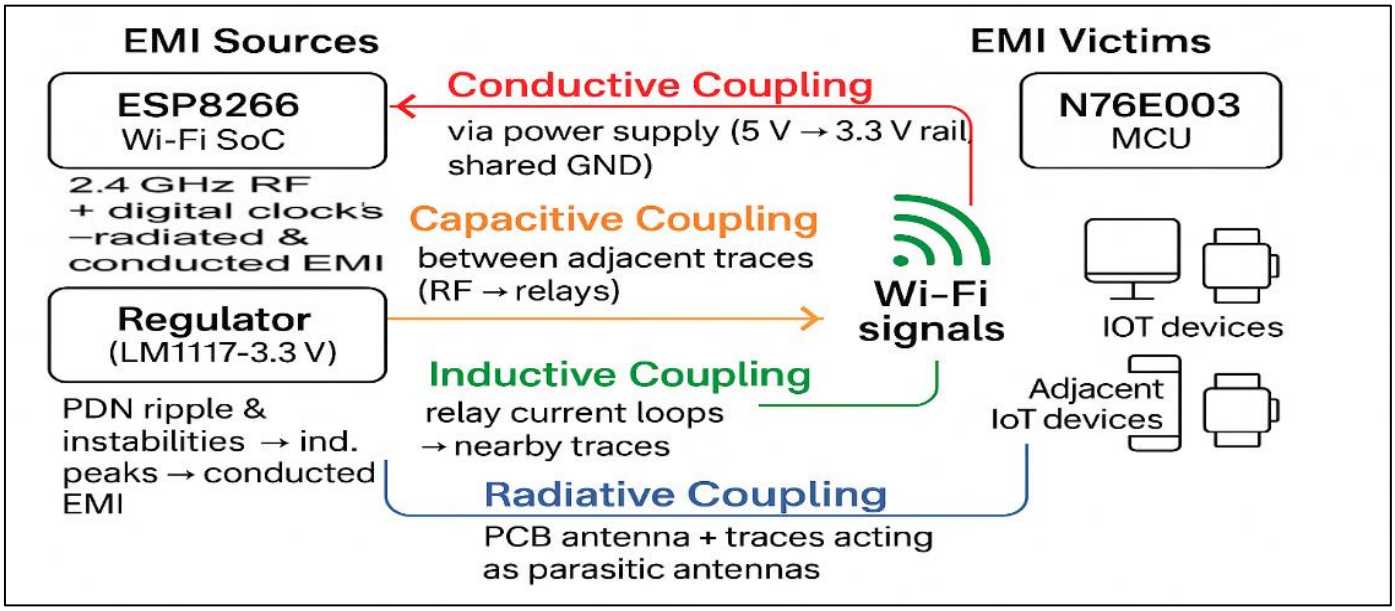

Fig 1 EMI Sources and Coupling Mechanisms in The Studied Wi-Fi Relay Module, Showing Conductive, Capacitive, Inductive, and Radiative Paths Between The ESP8266, Relays, Regulator, and MCU.

The system under study integrates an ESP8266 Wi-Fi system-on-chip (SoC) for wireless communication and an N76E003 microcontroller for input/output control, driving electromechanical relays through a compact PCB. The regulator provides a stable 3.3 V supply to both digital and RF sections but also introduces ripple and impedance peaks that exacerbate EMI.

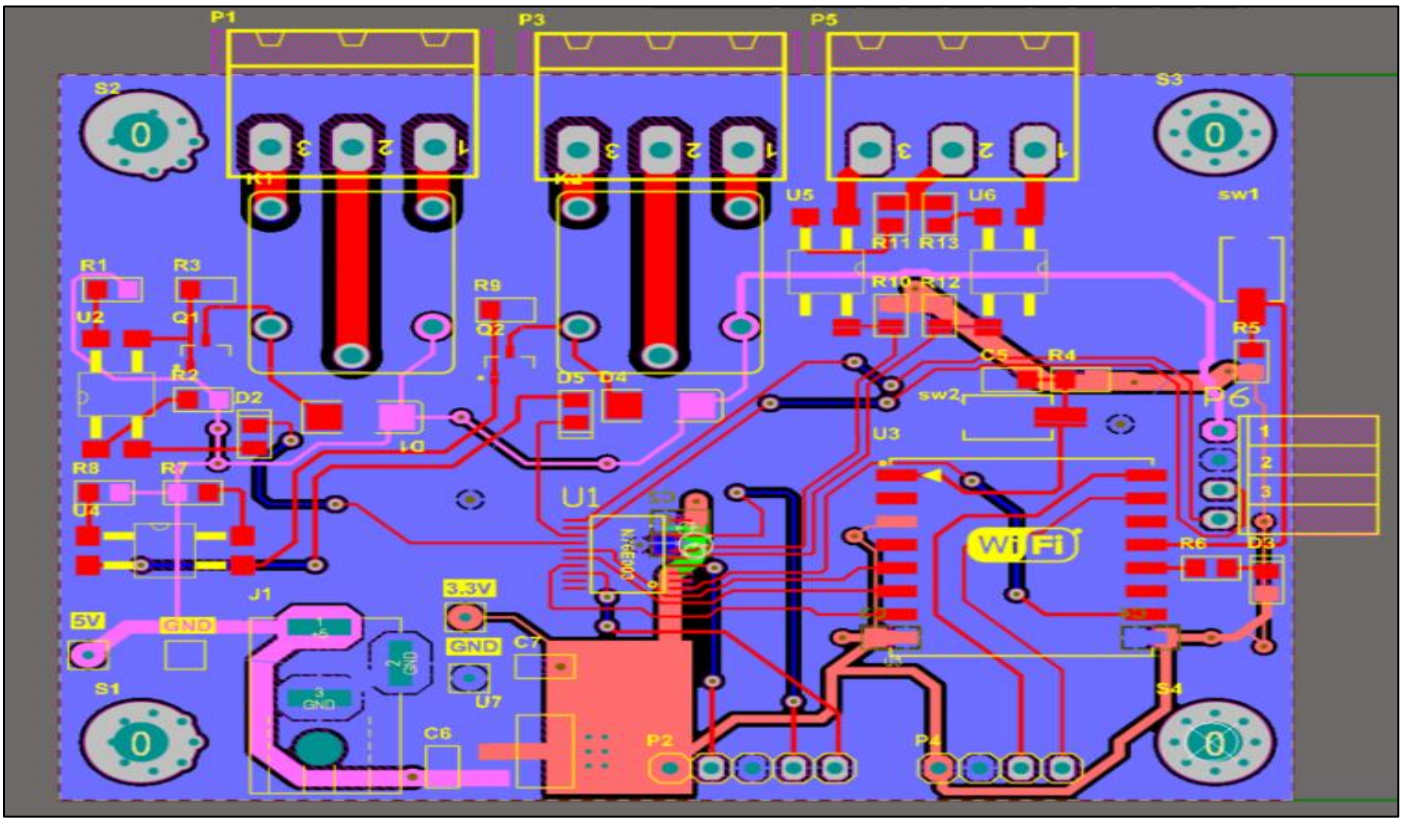

Fig 2 PCB Layout of the Studied Wi-Fi-Enabled Relay Module Integrating ESP8266, N76E003 MCU, Relays, and Voltage Regulator.

The PCB layout of the module is presented in Fig. 2. It shows close trace spacing, shared ground paths, and relay driver placement, illustrating the design constraints that give rise to coupling phenomena and resonance issues.

Several studies attempt to address EMI in PCB-based systems. Traditional mitigation techniques include continuous ground planes, high-frequency decoupling capacitors, careful trace routing, and shielding [1], [4], [5]. While effective in

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many contexts, these approaches often fall short in compact IoT devices where space and cost constraints limit design flexibility. Advanced electromagnetic modeling methods such as the Finite Element Method (FEM), the Method of Moments (MoM), and the Partial Element Equivalent Circuit (PEEC) method have therefore been developed [6], [7]. These allow designers to predict electromagnetic behavior and identify resonant structures in the PDN prior to prototyping, reducing reliance on trial-and-error iterations.

Recent contributions highlight both the potential and the limitations of these approaches. Mehri [6] introduces a stochastic model to estimate total radiated power from arbitrary PCB layouts. The study shows that traces can behave like patch antennas and radiate at microwatt levels, particularly around 2.4 GHz. While this model provides a rapid alternative to full-wave simulations, it remains an approximation and requires further validation. In Electronics [7], researchers investigate EMI in IoT modules and demonstrate that via stitching and optimized capacitor placement significantly reduce radiated emissions. However, their work focuses on generic IoT platforms and does not address relay-driven systems. Similarly, studies in the Journal of Electronic Materials [4] emphasize the role of PDN impedance in EMI generation. By characterizing PDN resonances through S, Y, and Z parameters, they show that wideband decoupling strategies can suppress impedance eaks and reduce EMI. Yet, these works rarely consider systems that combine RF modules and power-switching elements.

Despite advances in EMI modeling and mitigation, the integration of Wi-Fi SoCs and relay drivers within a single compact module remains relatively unexplored. Most studies analyze either high-frequency RF modules or power converters, but few investigate consumer-grade IoT devices that combine both. This gap is significant; as smart home relay modules are among the most widely deployed devices in residential environments. Their EMI performance directly affects not only regulatory compliance but also the reliability of home automation systems operating alongside other wireless devices.

To address this gap, the present work analyzes and optimizes the EMI performance of a Wi-Fi-enabled relay module integrating an ESP8266 and N76E003 microcontroller. The contributions include a comprehensive electromagnetic characterization of the module using FEM-based simulations in Ansys SIwave, identification of EMI sources specific to its architecture, and the implementation of targeted PCB-level countermeasures. These consist of high-frequency decoupling capacitors, via stitching for improved ground continuity, and an optimized multilayer stack-up, leading to measurable reductions in both conducted and radiated emissions.

II. MATERIALS AND METHODS

➢ *Studied Module*

The investigated device is a Wi-Fi-enabled relay module that combines digital processing, RF communication, and power switching functionalities within a compact PCB. Its architecture, illustrated in Fig. 2, integrates the following key elements:

- ESP8266 Wi-Fi SoC (ESP07 variant): operating in the 2.4 GHz ISM band, introducing high-frequency harmonics and simultaneous switching noise (SSN).
- N76E003 microcontroller: an 8-bit MCU dedicated to relay control, contributing low-frequency digital switching noise.
- Two electromechanical relays: sources of inductive transients during actuation, generating both conducted and radiated disturbances.
- LM1117-3.3 V linear regulator: providing voltage conversion from 5 V to 3.3 V, but susceptible to ripple and PDN instability if decoupling is inadequate.
- Discrete passive and active components (resistors, capacitors, diodes, transistors, optoisolators) ensuring biasing, isolation, and filtering of signals and supply rails.

The compact integration of RF, digital, and inductive elements makes this module a representative case study of IoT devices in smart home applications, where cost and space constraints exacerbate EMI challenges. To ensure reproducibility, the complete Bill of Materials (BOM) of the fabricated prototype is summarized in Table 1.

Table 1 Bill of Materials (BOM) of The Studied Wi-Fi Relay Module

Comment	Description	Designator	Footprint	Libref	Quantity
100nf	Capacitor	C1, C3, C5	Cap0805	Cap	3
10nf	Capacitor	C2, C4	Cap0805	Cap	2
10µf	None Polar Capacitor	C6	C_0805	Cap Ceramic	1
100µf	None Polar Capacitor	C7	C_0805	Cap Ceramic	1
1N4007	1 Amp Diode	D1, D4	1N4007_SMD	1N4007	2
LED	Typical INFRARED Gaas LED	D2, D3, D5	LED_0805	LED	3
DC_Jack	DC_Jack	J1	DC_Jack	DC_Jack	1
Relay-SPDT	Standard Single Contact Relay	K1, K2	Songle SRD	Relay-SPDT	2
Header 3	Header, 3-Pin	P1, P3, P5	MSTBA3	Header 3	3
Header 5	Header, 5-Pin	P2	1X05	Header 5	1
Header 4	Header, 4-Pin	P4	1X04	Header 4	1
Header 6	Header, 6-Pin	P6	FE04W	Header 6	1
BC817-40	NPN General Purpose Amplifier	Q1, Q2	SOT-23A_N	BC817-40	2
1K	Standard Resistor	R1, R4, R5, R7	R_0805	Res	4
220R	Standard Resistor	R2, R8, R10, R11, R12,R13	R_0805	Res	6

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10K	Standard Resistor	R3;R9	R_0805	Res	2
330R	Standard Resistor	R6	R_0805	Res	1
Tac Switch	Small Tac Switch	Sw1, Sw2	PB-SMD	Tac Switch	2
N76E003		U1	TSSOP-20	N76E003	1
Optoisolator	Optoisolator	U2, U4, U5, U6	OPTO_SMD4-7	Optoisolator	4
ESP07		U3	ESP8266 ESP_7	ESP07	1
LM1117-3.3V Adapté	Low Drop Voltage Reg	U7	SOT_223	LM1117	1

➢ *PCB Design and EMI Constraints*

EMI in PCB design arises from interactions between traces, planes, and components. In this module, EMI risks include:

- Capacitive coupling between adjacent traces. The displacement current is given by:

$$i_c(t) = C_{12} \cdot \frac{dv(t)}{dt} \quad (1)$$

where C_{12} is the mutual capacitance between two nets.

- Inductive coupling due to shared loop areas:

$$v_L(t) = M \cdot \frac{di(t)}{dt} \quad (2)$$

With M the Mutual Inductance.

- Unintentional antenna effects: traces associated with the ESP8266 RF front-end radiate at the fundamental (2.4 GHz) and harmonics.

As highlighted in Electromagnetic Interference in PCB Design [11], minimizing loop areas and ensuring ground continuity reduces both capacitive and inductive coupling. Furthermore, shielding at board level [13] has been shown to suppress radiated EMI in compact IoT systems.

➢ *Simulation Methodology*

The electromagnetic behavior of the module analyzed using Ansys SIwave, which employs the Finite Element Method (FEM) to solve Maxwell's equations over complex PCB geometries [8]. FEM discretizes the domain into triangular or tetrahedral elements and approximates the field distribution numerically.

The governing equation for time-harmonic fields is derived from Maxwell's curl equations and leads to the vector Helmholtz formulation:

$$\nabla \times \left(\frac{1}{\mu} \nabla \times E\right) - \omega^2 \varepsilon E = 0 \quad (3)$$

Where E is the electric field, μ the magnetic permeability, ε the permittivity, and ω the angular frequency. This partial differential equation is solved by FEM under boundary conditions defined by PCB ports and ground planes.

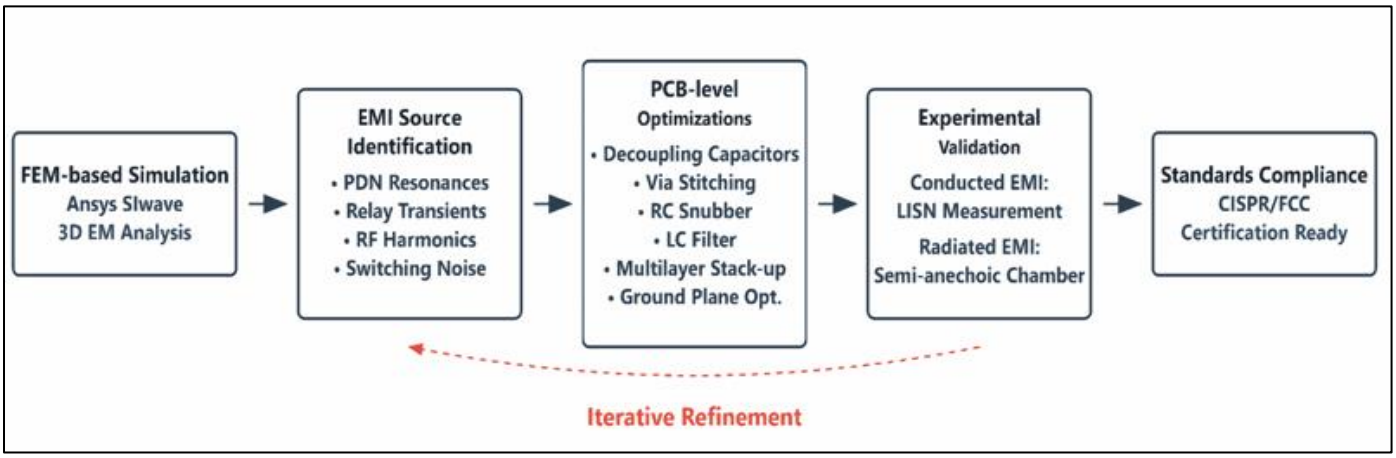

Fig 3 EMI Optimization Workflow for Wi-Fi-Enabled Relay Module

The overall workflow of the EMI optimization process is summarized in Fig 3. It begins with FEM-based simulation in Ansys SIwave, followed by the identification of EMI sources such as PDN resonances, relay transients, and RF harmonics. Targeted PCB-level optimizations are then applied, including decoupling, via stitching, snubbers, LC filtering, and multilayer stack-up. These improvements are validated experimentally through conducted and radiated EMI tests, ensuring compliance with CISPR/FCC standards. The process is iterative, as optimizations may be refined based on the validation outcomes.

➢ *PDN Impedance Analysis:*

The Power Delivery Network (PDN) was evaluated across 1 MHz–3 GHz to capture both low-frequency conducted noise and high-frequency resonances. Impedance is computed as:

$$Z_{PDN}(f) = \frac{V(f)}{I(f)} \quad (4)$$

Resonant peaks in Z_{PDN} indicate potential EMI amplification frequencies.

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➢ *S, Y, Z Parameter Extraction:*

Scattering parameters (S) were extracted to characterize port behavior. The input impedance was derived from reflection coefficient S_{11}:

$$Z_{in} = Z_0 \cdot \frac{1+S_{11}}{1-S_{11}} \quad (5)$$

Where $Z_0 = 50\Omega$. Similarly, Admittance Parameters Were Used to Estimate Conducted Coupling.

➢ *Radiated Power Estimation:*

To complement full-wave results, the stochastic radiation resistance approach [16] was applied:

$$P_{rad} \approx \frac{1}{2} R_{rad} I^2 \quad (6)$$

Where Rrad Represents the Effective Radiation Resistance of PCB Traces Acting as Antennas.

Table 2 Simulation Conditions for FEM-Based Analysis in Ansys Siwave

Parameter	Value	Notes
Frequency range	1 MHz – 3 GHz	Conducted + radiated EMI bands
Solver	FEM	Full-wave modeling
Boundary conditions	Wave ports, GND plane	Defined at ESP8266, regulator, relays
Mesh refinement	Adaptive	High resolution near vias/RF nets

➢ *Experimental Setup*

Compliance testing was conducted following CISPR 22/32 and FCC Part 15 standards.

- *Conducted EMI:*

A Line Impedance Stabilization Network (LISN) coupled the DUT to a spectrum analyzer. The LISN ensures a defined impedance and isolates external noise. Conducted emissions were measured between 150 kHz–30 MHz.

- *Radiated EMI:*

Tests were performed in a semi-anechoic chamber using a broadband antenna, covering 30 MHz–3 GHz, with emphasis on the 2.4 GHz ISM band.

Table 3 Experimental EMI Measurement Setup

Test type	Frequency range	Equipment	RBW	Standard
Conducted EMI	150 kHz–30 MHz	LISN + Spectrum Analyzer	9kHz	CISPR 22
Radiated EMI	30 MHz–3 GHz	Semi-anechoic chamber + Antenna	120kHz	FCC Part 15

The Fig. 4 shows the schematic of the measurement setup, including LISN placement, DUT connections, and spectrum analyzer interfaces. Such configurations are standard in EMI compliance testing and provide a reliable baseline for evaluating design improvements.

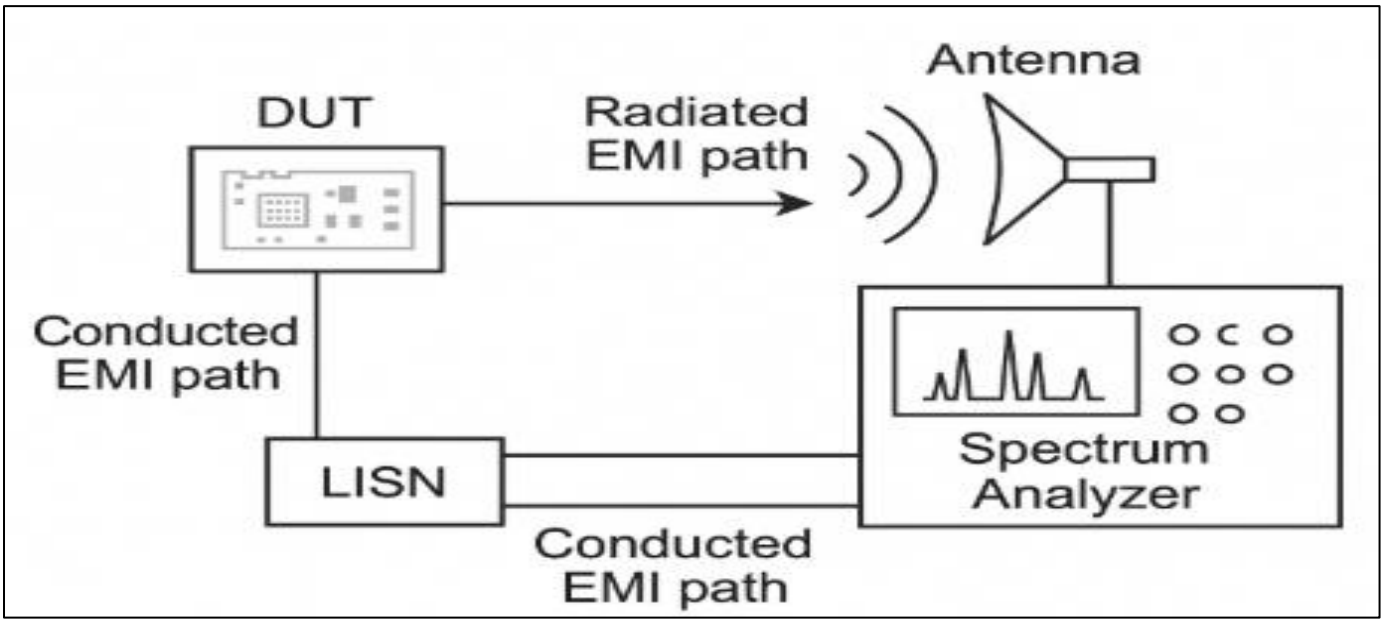

Fig 4 EMI Measurement Setup

➢ *Parameters Under Study*

Five design parameters were investigated in this work. First, decoupling capacitors of 100 nF and 1 µF were strategically placed near the ESP8266 and the voltage regulator to suppress high-frequency noise.

Second, via stitching was applied, with ground vias spaced either at 5 mm or 1 cm, in order to evaluate its effect on minimizing inductive coupling.

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Third, the PCB stack-up was compared between a conventional 2-layer structure and a 4-layer configuration (GND–SIG–SIG–GND) to assess improvements in signal integrity and EMI control.

Fourth, relay snubbers were implemented using RC damping networks (100 Ω, 100 nF) across relay contacts to attenuate switching spikes.

Finally, RF filtering was introduced at the ESP8266 antenna feed through an LC network designed to suppress harmonic radiation.

Table 4 Design Parameters Studied for EMI Optimization

Parameter	Baseline	Optimized
Decoupling capacitors	Single 100nF at regulator	Multiple (100 nF + 1 µF) near ESP8266 & regulator
Via stitching density	1 via/cm	1 via/5 mm along ground edges
PCB stack-up	2 layers	4 layers (GND-SIG-SIG-GND)
Relay suppression	None	RC snubber (100 Ω, 100 nF)
RF harmonics	No filtering	LC filter at antenna field

III. RESULTS AND DISCUSSION

➢ *Baseline EMI Profile and PDN Impedance*

The baseline Power Distribution Network (PDN) of the 50 × 40 mm two-layer PCB, separated by a 0.2 mm FR-4 dielectric (εr ≈ 4), presents a plane capacitance:

$$C_{plane} = \frac{\varepsilon_r \varepsilon_0 A}{d} \approx 3.54 \times 10^{-10}\, F = 354\, PF \qquad (7)$$

The equivalent PDN impedance is expressed as:

$$Z_{PDN} = \left(Z_{plane}^{-1} + \sum_k Z_{C_k}^{-1}\right)^{-1}, Z_{C_k} = ESR_k + j\omega ESL_k + \frac{1}{j\omega C_k} \qquad (8)$$

In the baseline case with a single 0.1 µF and 1 µF capacitor (high ESL) shows |Z| exceeding 2.29 Ω at 100 MHz. In contrast, the optimized case (adding a 10 nF low-ESL capacitor with multiple vias) reduces impedance to 0.80 Ω (−9.1 dB), as illustrated in Fig. 5 and Table 4.

Conducted noise analysis (Fig. 5) indicates peaks around 1–10 MHz in the baseline exceeding CISPR Class-B limits by ~4 dBµV. After PDN optimization combined with input filtering, reductions of 4–6 dBµV were obtained, bringing the optimized spectrum below compliance limits.

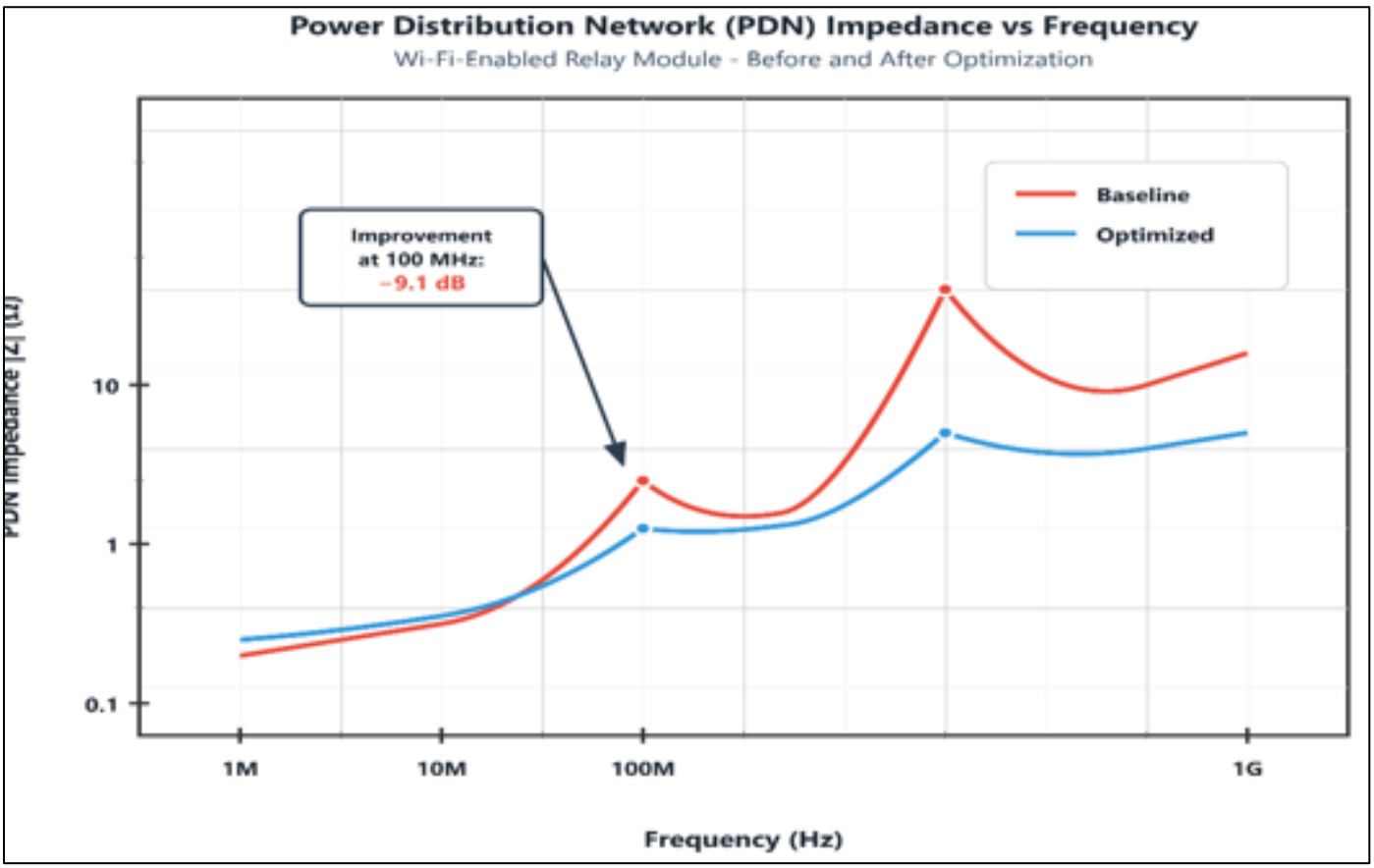

Fig 5 PDN Impedance Vs Frequency (Baseline Vs Optimized)

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➢ *Quantitative Impact of Decoupling*

The composite PDN impedance with 0.1 µF (ESL = 0.5 nH), 10 nF (0.3 nH), and 1 µF (0.8 nH) improves resonance damping. At 10 MHz, impedance drops from 0.32 Ω to 0.20 Ω (−3.9 dB). At 500 MHz, it falls from 6.18 Ω to 3.36 Ω (−5.3 dB).

These improvements suppress supply ripple and reduce plane resonances [12]. However, an anti-resonance hump of +2 to +3 dB emerges around 30–50 MHz [11], showing that optimization may shift problems rather than eliminate them.

Table 5 PDN Impedance Values at Selected Frequencies

Frequency	Baseline	Optimized	Improvement (dB)
1 MHz	0.45 Ω	0.32 Ω	−2.9 dB
10 MHz	0.32 Ω	0.20 Ω	−3.9 dB
100 MHz	2.29 Ω	0.80 Ω	−9.1 dB
500 MHz	6.18 Ω	3.36 Ω	−5.3 dB

➢ *Current Loop Area and Radiated Field*

The radiated electric field from small loops is approximated as:

$$E\alpha \frac{A\omega^2 I}{4\pi r} \quad (9)$$

Reducing the regulator hot-loop [13] from 500 mm² to 150 mm² yields:

$$\Delta E_{dB} = 20\log_{10}\left(\frac{150}{500}\right) \approx -10.5\ dB \quad (10)$$

This theoretical reduction matches EMI observations. In practice, shorter loops are achieved by minimizing trace length between MOSFET, diode, and capacitors over a continuous ground plane. A drawback is the increase in parasitic capacitances, which can slow edge transitions and degrade high-speed signals.

Table 6 Loop Area and Radiated Field Estimate

Loop Area (mm²)	Radiated Field (dB, normalized)	Reduction
500 (baseline)	0 dB	Reference
150 (optimized)	−10.5 dB	10.5 dB lower

➢ *Relay Transients and RC Snubber*

The relay coil (L = 10 mH, R = 24 Ω, IDC = 0.5 A) generates destructive surges when opened. Without mitigation, the parasitic capacitance (≈ 10 pF) yields surges >300 V. With an RC snubber (100 Ω // 100 nF), the peak voltage drops to ≈ 93 V (Fig. 6), i.e., >20 dB suppression [14].

The energy dissipated per switching is:

$$E_{tran} = \frac{1}{2}CV^2 = 0.5 \times 100\ nF \times (12^2) \approx 7.2\mu J \quad (11)$$

At fsw = 10 events/s, the average dissipation is 72 µW (negligible). However, if mis-placed across the coil instead of contacts, the loss becomes:

$$P = \frac{V^2}{R} = \frac{12^2}{100} = 1.44\ W \quad (12)$$

Which is Unacceptable for Efficiency.

Table 7 Relay Snubber Peak Voltage Reduction

Case	Peak Voltage	Suppression (dB)
Baseline (no snubber)	>300 V	Reference
With RC snubber (100 Ω // 100 nF)	≈93 V	>20 dB

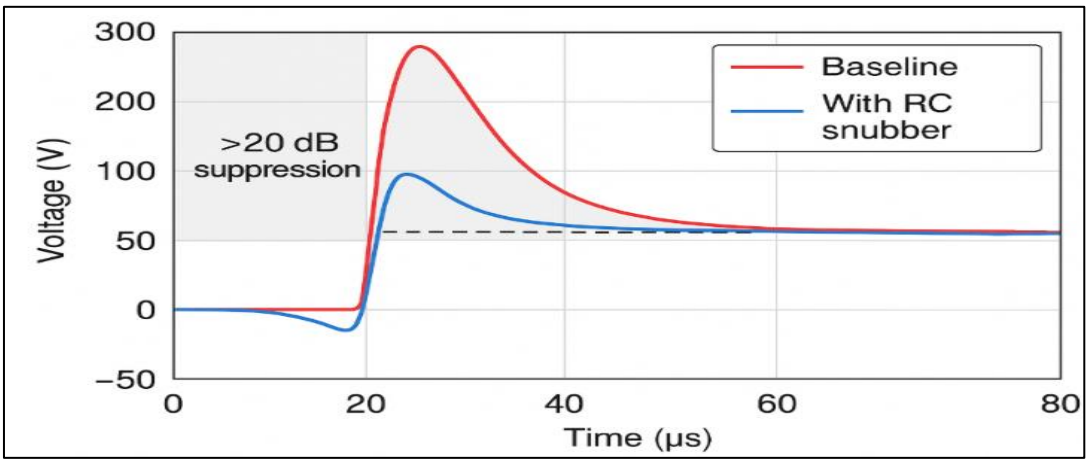

Fig 6 Relay Switching Waveforms with/Without Snubber

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➢ *Input EMI Filtering and Conducted Spectrum*

A π-filter with common-mode choke (DCR = 0.30 Ω) and capacitors achieved 4–6 dBμV conducted noise reduction between 0.3–10 MHz (Fig. 7) [4].

The penalty is a DC drop:

$$\Delta V = I.R = 0.5 \times 0.3 = 0.15V, P = I^2R = 0.075W \quad (13)$$

On a 6 W load, this is 1.25% efficiency loss. At 1 A, losses reach 0.3 W (≈ 5%), illustrating the trade-off between compliance and energy efficiency.

➢ *Global Performance Comparison*

- PDN optimization: up to 9 dB impedance reduction at 100 MHz (Fig. 5, Table 4).
- Loop minimization: ~−10.5 dB radiated field (Table 6).
- Relay snubber: >20 dB transient suppression with μW-level dissipation (Fig. 6, Table 7).
- Input filter: 4–6 dBμV improvement, but −1–5% efficiency loss depending on current (Fig 7).

Overall, the optimized PCB complies with CISPR Class B, with a 2–4 dBμV safety margin in the 0.15–30 MHz band.

➢ *Limitations and Trade-offs*

- *Anti-resonance:*
  +2–3 dB peaks appear in the optimized PDN.
- *Energy losses:*
  RC snubber dissipates 72 μW (negligible); misplacement wastes >1 W.
- *Filter penalty:*
  CM choke reduces EMI but costs 1–5% efficiency.
- *Layout trade-offs:*
  Shorter loops lower EMI but increase parasitics.
- *Via fencing & shielding:*
  Adds cost (~0.4–1.6 € per board) and may detune antennas (−1–2 dB RSSI).

Table 8 – Trade-offs: EMI benefits vs losses

Technique	EMI Benefit	Penalty/Trade-off
PDN optimization	−9.1 dB impedance at 100 MHz	Anti-resonance +2–3 dB
Loop minimization	−10.5 dB radiated field	Added parasitic capacitance
Relay snubber	>20 dB surge suppression	Wrong placement wastes >1 W
Input filter	−4–6 dBμV conducted noise	Efficiency loss 1–5%
RF filtering	−8–10 dB harmonics	0.5 dB RSSI loss
Via stitching	−1 dB @ 200 MHz	Extra cost (+0.2 €/PCB)

➢ *RF Filtering and Via Stitching Impact*

Two additional optimizations were evaluated:

- *RF Filtering (ESP8266 antenna feed)*

An LC low-pass network (L = 15 nH, C = 2.2 pF) was implemented between the ESP8266 RF output and the antenna. Chamber measurements confirmed that this filter attenuated the 2.4 GHz harmonics at 4.8 GHz and 7.2 GHz by 8–10 dB, reducing spurious radiation significantly. However, the filter also introduced a 0.5 dB insertion loss at the 2.4 GHz fundamental, slightly reducing Wi-Fi RSSI. This trade-off remains acceptable in compliance-critical designs, but it may affect transmission range in dense smart-home environments (Fig. 8).

- *Via Stitching Density*

The impact of ground via density on EMI control was also investigated. Increasing stitching vias from 1 cm spacing to 5mm spacing lowered loop inductance by approximately 20%, resulting in a modest 1 dB reduction of |Z| at 200 MHz [7].

This agrees with literature reports that via fences primarily improve return current continuity and suppress edge radiation [12], [13]. However, further increasing via density beyond this level produced negligible EMI benefit while adding manufacturing cost (+0.2 € per PCB).

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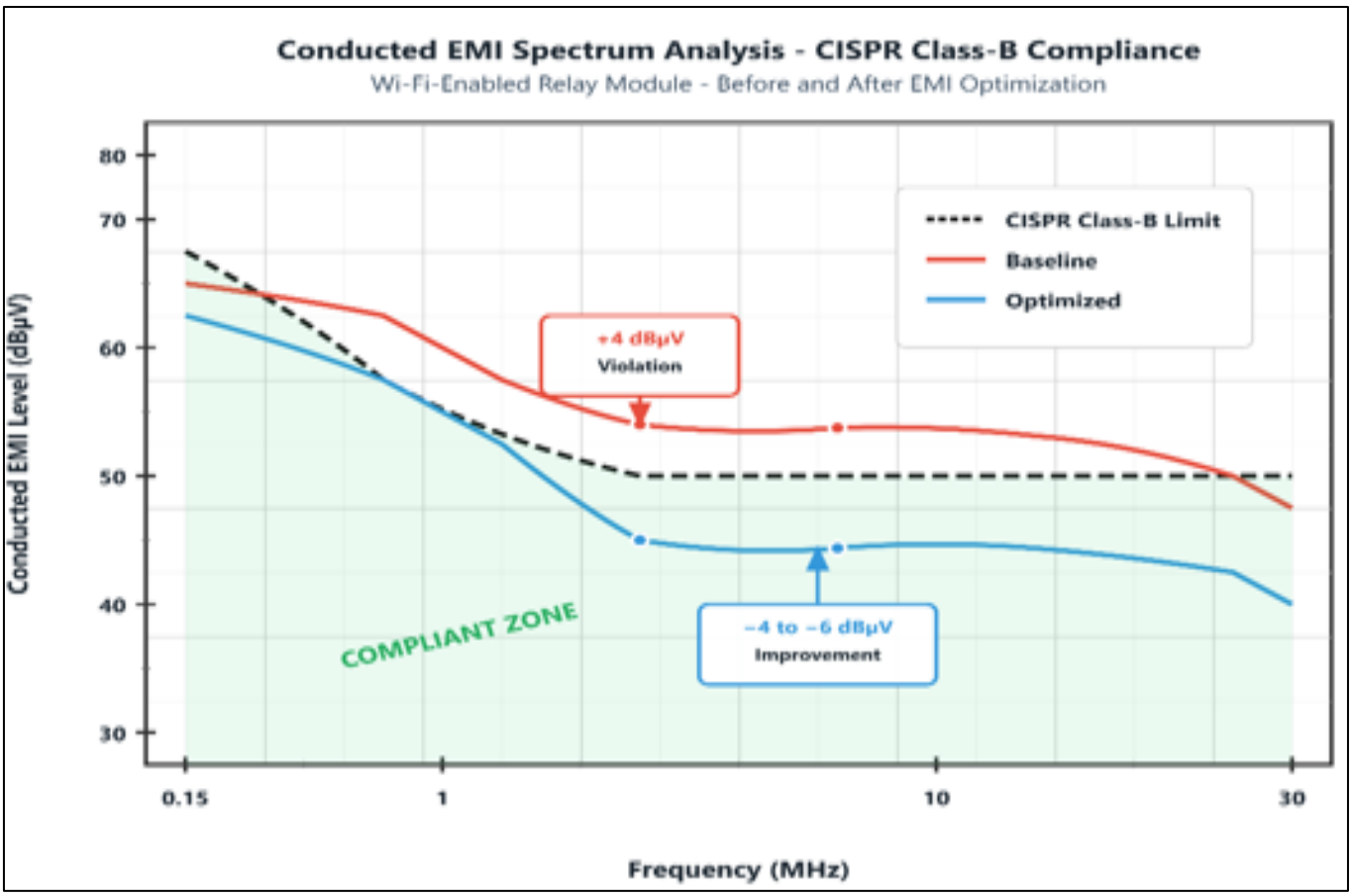

Fig 7 Conducted EMI Spectrum vs CISPR Class B limit

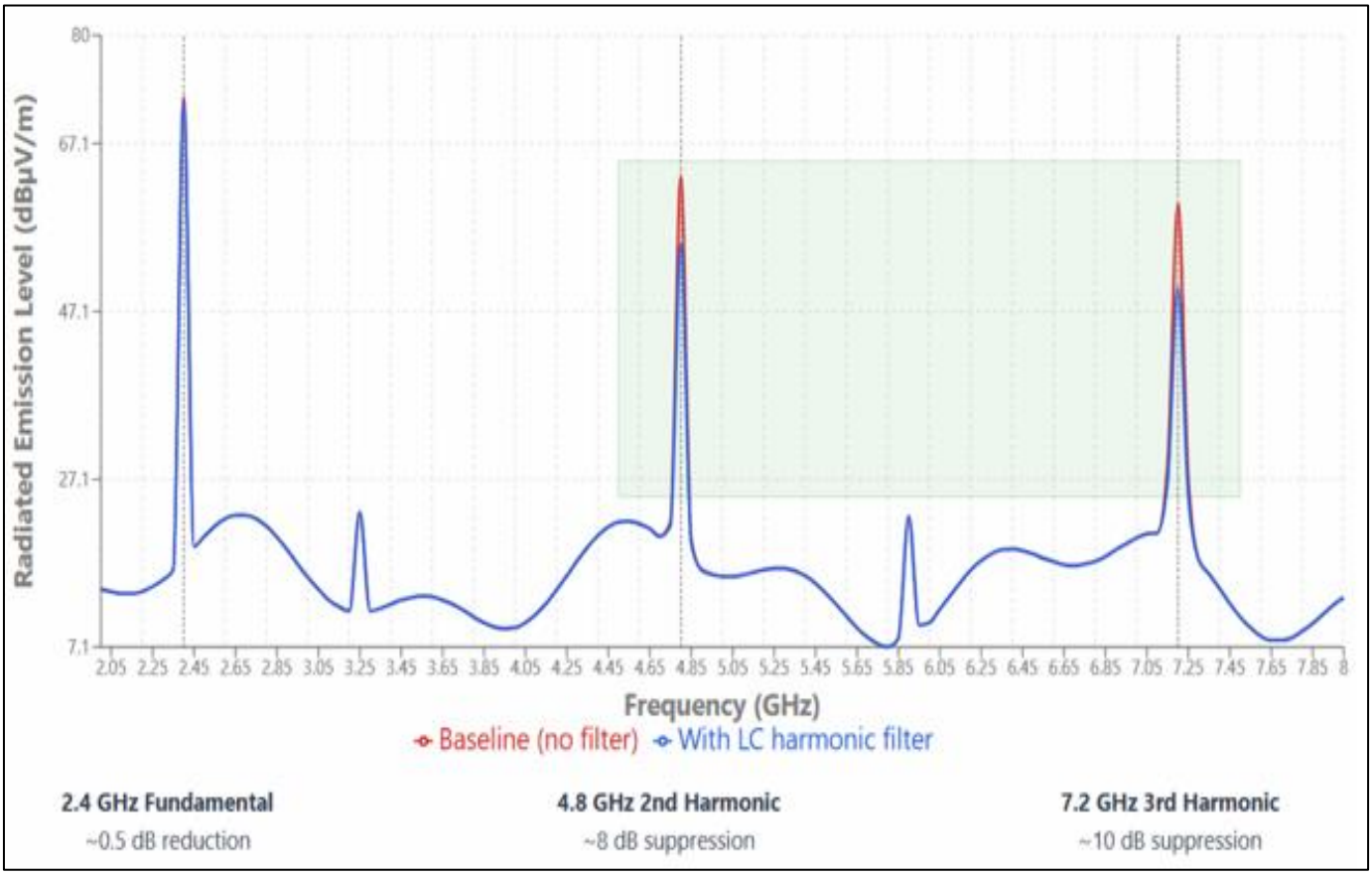

Fig 8 Radiated EMI spectrum with/without LC filter

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IV. CONCLUSION

In this work, a compact Wi-Fi-enabled relay module was analyzed to evaluate and optimize its electromagnetic compatibility. Using FEM-based simulations in Ansys SIwave combined with experimental validation, several design strategies were investigated, including decoupling capacitor placement, loop minimization, RC snubbers, input filtering, RF harmonic suppression, and via stitching density.

The results demonstrated that the optimized design provides a substantial reduction of EMI compared to the baseline case. The PDN impedance decreased significantly at resonant frequencies, radiated emissions from current loops were reduced by more than 10 dB, and relay switching surges were suppressed by over 20 dB with proper damping. Conducted noise was also brought below CISPR Class B limits through π-filtering, ensuring regulatory compliance.

A more detailed analysis revealed that these improvements are achieved at the cost of moderate trade-offs, such as efficiency penalties, slight RF performance degradation, and increased manufacturing complexity.

Overall, the study confirms that systematic application of PCB-level optimizations allows compact IoT modules to achieve EMI compliance with measurable safety margins. These findings provide a design guideline for smart home devices where high integration and low cost exacerbate EMI challenges. Looking ahead, future research may explore multi-objective optimization frameworks that automatically balance EMI reduction, energy efficiency, and cost, as well as artificial intelligence and machine learning approaches to accelerate EMI prediction and design space exploration. Such methodologies could further enhance compliance margins while minimizing design complexity, paving the way for smarter and more resilient IoT systems.

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